

OPERATING AND SERVICE MANUAL

12607

DIRECT MEMORY ACCESS

(2114B COMPUTER ACCESSORY KIT)

Note

This manual should be retained with the Installation and Maintenance Manual (part no. 02114-90399) for the HP 2114B Computer.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the optional Hewlett-Packard 12607A Direct Memory Access (DMA) Accessory Kit.

1-3. GENERAL DESCRIPTION.

1-4. The DMA option is used with the HP 2114B general purpose computer. The DMA option consists of a single plug-in card, which plugs into a prewired slot in the computer. DMA is single-channelled and is program-assignable to addresses 10 through 16. The HP 12607A DMA Accessory Kit includes the following items:

- a. 12607-6001 Single-Channel DMA Card.
- b. 12607-90002 DMA Operating and Service Manual and Diagnostic Supplement.
- c. HP 20524A (or later) DMA Binary Diagnostic Tape.
- d. HP 20525A (or later) DMA Binary Rate and Transfer Diagnostic Tape.

1-5. DMA enables the computer to transfer data directly between memory and external devices at a maximum rate of 500,000 16-bit words per second in block lengths of 1 to 8192 words. Word transfer time is 2.0 microseconds for each 16-bit word. No character packing hardware is provided on the card; when using byte (eight bit) oriented devices, character packing and unpacking may be accomplished with software, before or after data transfer.

1-6. To be placed in operation, the DMA system must first be initialized for a specific operating mode by instructions and control words in the main program. Data interchange then occurs automatically when a service request signal is received from an I/O channel programmed to DMA. The DMA option then takes control of the central processor and I/O system, suspends the running program at the end of the current phase, and during the following machine cycle, generates a special phase 5 memory cycle to read or write a word directly into or out of a predetermined memory location. At the end of the phase 5 memory cycle (one complete machine cycle), control is returned to the central processor and I/O system, and the main program is automatically resumed at the point where it was suspended, without loss of continuity. A new phase 5 cycle is initiated each time the I/O device signals DMA that it is ready to input or output another word. When all data in a predetermined block length have been transferred, DMA initiates a normal interrupt to a service subroutine.

1-7. IDENTIFICATION.

1-8. Printed-circuit card revisions are identified by a letter and a date code stamped on the card. The letter code identifies the version of the etched trace pattern on the unloaded card. The date code refers to the electrical characteristics of the loaded card. If the date code stamped on the printed circuit card does not agree with the date code shown on the schematic diagram in section IV of this manual for the DMA card, there are differences between your card and the card described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section contains installation and programming information for the DMA option, including program word formats and a typical DMA program.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the card is unpacked. Inspect the card for damage (cracks, broken parts, etc.). If the card is damaged or fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged card without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. No special installation procedures are required to install the DMA option. However, make certain that power is off at the computer before plugging the DMA card into connector XA16 in the computer mainframe. After the DMA card has been installed, perform diagnostic test procedures contained in the diagnostic supplement to this manual to ensure proper operation of the DMA card.

2-7. PROGRAM WORD FORMATS.

2-8. The DMA option is programmed using HP assembler language. The instruction, control, and data word formats used in the operation of DMA are shown in figure 2-1 and are defined below.

a. Input/output instruction words: I/O group instructions addressed to select code 2 or 6 that permit the central processor to control the following DMA functions through the I/O select codes specified:

- (1) Select code 2 permits initialization channel control flip-flop on DMA card to be addressed by CLC and STC instructions.
- (2) Select code 2 preceded by a CLC instruction permits DMA memory address register to be addressed by an OTA instruction.
- (3) Select code 2 preceded by a STC instruction permits DMA word count register to be addressed by OTA and LIA instructions.

- (4) Select code 6 permits DMA switching functions to be addressed by OTA, CLC, STC, CLF, STF, SFC, and SFS instructions.

b. DMA program control words: Program constants that can be programmed to DMA to specify the following information:

- (1) The I/O channel select code address of the device to be serviced by DMA (bits 0 through 2 select devices 10 through 16).
- (2) Clear (turn off) control on device after last word in data block has been transferred (bit 13 = 1).
- (3) Do not clear control on device after data transfer (bit 13 = 0).
- (4) Set (turn on) control on device after each word in data block has been transferred (bit 15 = 1).
- (5) Do not set control on device after each transfer (bit 15 = 0).

c. DMA address words: Program constants that can be programmed to DMA to specify the following information:

- (1) Starting memory address for first word of input/output data block (bits 0 through 14).
- (2) Memory input from device I/O channel (bit 15 = 1).
- (3) Memory output to device I/O channel (bit 15 = 0).

d. DMA block length words: Program constants that can be programmed to DMA to specify the number of words in the data block. Word count is a number expressed as the two's complement of the positive binary equivalent of the number.

e. Data input/output words: Format used to transfer data directly between the device I/O channel and memory.

2-9. TYPICAL DMA PROGRAM.

2-10. An example of a typical program that uses the DMA option is listed in table 2-1. In this program, a memory input operation is carried out where a block of 50₁₀ words is read from a tape reader (I/O channel select code address 10₈) into computer memory locations 200₈ through 261₈.

INPUT/OUTPUT INSTRUCTION WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO GROUP						INSTRUCTION				SELECT CODE 2 OR 6					

DMA PROGRAM CONTROL WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\frac{1}{0}$ STC	NOT USED	CLC	NOT USED										DEVICE SELECT CODE		
STC		CLC													

DMA ADDRESS WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\frac{1}{0}$ IN	NOT USED		WORD ADDRESS												
OUT															

DMA BLOCK LENGTH WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED			WORD COUNT												

DATA INPUT/OUTPUT WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16 - BITS															

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Figure 2-1. DMA Instruction and Control Word Formats

Note

The program in table 2-1 assumes that the interrupt system is enabled (STF0

instruction) and that DMA will initiate an interrupt to a service subroutine when all words in the assigned data block have been transferred.

Table 2-1. Typical DMA Program

LABEL	OP CODE	OPERAND	REMARKS
<u>INITIALIZE DMA FOR INPUT</u>			
ASGN	LDA	CW1	Fetches control word 1 (CW1) from memory and loads it in A-register.
	OTA	6	Outputs CW1 to DMA.
MAR	CLC	2	Prepares DMA memory address register to receive and store control word 2 (CW2).
	LDA	CW2	Fetches CW2 from memory and loads in in A-register.
	OTA	2	Outputs CW2 to DMA.
WCR	STC	2	Prepares DMA word count register to receive and store control word 3 (CW3).
	LDA	CW3	Fetches CW3 from memory and loads it in A-register.
	OTA	2	Outputs CW3 to DMA.
<u>START DEVICE AND DMA</u>			
STRT	STC	10B,C	Initiate tape reader data transfer.
	STC	6B,C	Activate DMA.
<u>DMA DATA TRANSFER</u>			
	.	.	Continue program while data transfer takes place.
	.	.	
	.	.	
<u>DMA CONTROL WORDS</u>			
CW1	OCT	120010	Assignment for DMA; specifies I/O channel select code address (10g), STC after each word is transferred, and CLC after final word is transferred.
CW2	OCT	100200	Memory address register control for DMA; specifies memory input operation and starting memory address (200g).
CW3	DEC	-50	Word count register control for DMA; specifies the two's complement of the number of words in the block to be transferred.

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section contains a brief functional description and a detailed circuit description for the DMA option.

Note

For a description of abbreviations (mnemonics) used in this section, refer to table 4-1.

3-3. FUNCTIONAL DESCRIPTION.

3-4. The DMA option adds a fifth phase to the four-phase capability of the basic computer. Phase 5 is a special memory cycle that requires one machine timing cycle (T0 through T7). Once initiated by service request signals received from I/O channels programmed to DMA, phase 5 operation is automatic and independent of program control. Each phase 5 cycle permits one input or output word to be exchanged between an external device (tape reader, disc memory, magnetic tape unit, etc.) and computer memory.

3-5. When a service request is received by DMA, the main program is suspended for one machine cycle to achieve data transfer (one 16-bit word per cycle), rather than achieving data transfer by interrupting to a service subroutine. While the program is suspended, the computer is in phase 5 and data is transferred to or from the external device. At the end of the phase 5 cycle, the main program (now delayed by one machine cycle) continues from the point that it was suspended since the counting registers in the central processor are not stepped during a phase 5 cycle. A DMA interrupt occurs only after the word count function signals that all words in a data block have been transferred.

3-6. Figure 3-1 is a functional block diagram showing the relationship between the HP 2114B logic circuitry and the DMA logic. Table 3-1 lists the step-by-step sequence for DMA operation. When referencing figure 3-1 and table 3-1, assume that the typical DMA program in table 2-1 is being run. Since this program is for a memory input operation, table 3-1 does not cover the sequence for a memory output operation. However, the two operations are the same except for the signals generated to transfer data between the IOB lines and memory. These signals are shown for both operations in figure 3-1.

3-7. DETAILED CIRCUIT DESCRIPTION.

3-8. The following paragraphs contain a detailed circuit description for the DMA option. The description

covers initialization, generation of a phase 5 signal, data input and output operations, DMA register stepping and device turn-off, and DMA completion interrupt. See the schematic diagram for DMA (figure 4-1) whenever referring to this circuit description.

3-9. INITIALIZATION

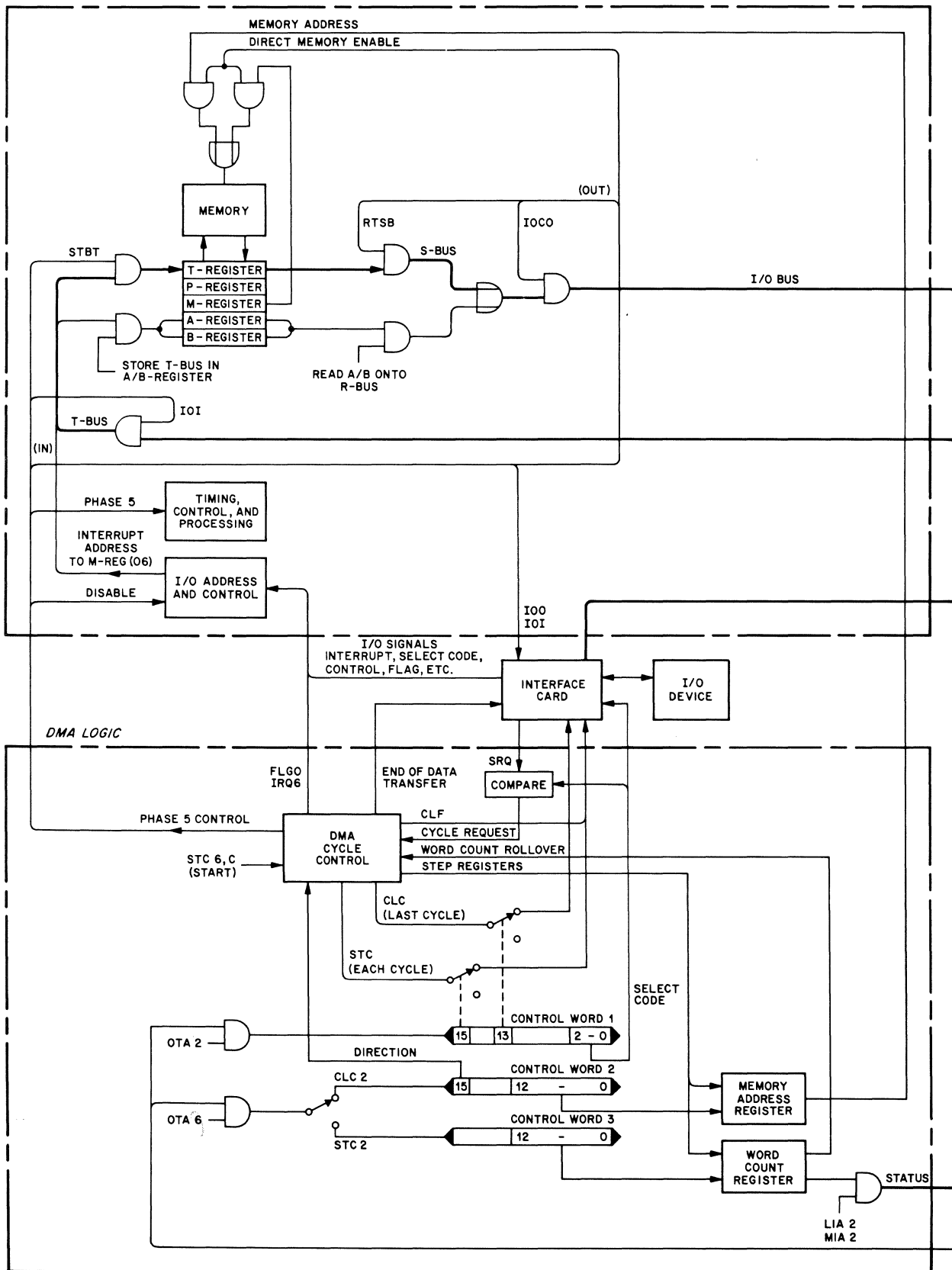
3-10. When the DMA option is initialized, the first control word is output to the DMA card on the IOB lines with an OTA 6 instruction in the main program. At T3T4, bits 0, 1, and 2 are clocked into service select register FF's MC55A, MC55B, and MC55C. The bits are encoded by MC76 to provide the least significant octal digits of the select code of the external device involved in the data transfer. This information will remain on the service select (SS) lines until the data transfer is complete and a succeeding data transfer is initiated. Bit 13 of the first control word sets the clear control FF if the bit is true and a true bit 15 sets the set control FF. These flip-flops are clocked at T3T4 when the SC6 signal and the IOO signal are both true.

3-11. The second step in initializing DMA is to output a CLC 2 instruction which resets the initialization channel control FF. The second control word may then be loaded into the A-register and output to DMA over the IOB lines by a OTA 2 instruction. Bits 0 through 12 of control word 2 specify the starting address of the block of data to be transferred, and bit 15 specifies whether the data transfer is an input or an output operation (bit 15 = logic 1 = input operation). At T3T4 the IOO signal is true, making all inputs to MC14C true, and a false $\overline{\text{LMAR}}$ signal is generated. The false $\overline{\text{LMAR}}$ signal allows the starting address on the IOB lines to be clocked into the memory address register, and the address appears on lines XMR0 through XMR12. At the same time, bit 15 is clocked into the memory address register and pin 7 of MC75 goes true for a data input operation or false for an output operation.

3-12. Next, an STC 2 instruction is output to DMA which sets the initialization control FF. Control word 3 is then loaded into the A-register and output to DMA on the IOB lines, again by an OTA 2 instruction. Bits 0 through 12 of control word 3 specify the 2's complement of the number of words in the data block to be transferred. At T3T4, all inputs to MC14B are true and a false $\overline{\text{LWCR}}$ signal is generated. The false $\overline{\text{LWCR}}$ signal clocks bits 0 through 12 of control word 3 into the word count register. The word count register output lines (WCR0 through WCR12) now reflect the 2's complement of the number of words in the data block.

3-13. An IOI signal (resulting from an LIA, LIB, MIA, or MIB instruction) will cause the WCR bits to be read onto

COMPUTER LOGIC



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Figure 3-1. DMA Functional Block Diagram

Table 3-1. Basic Sequence for DMA Data Transfer

INITIALIZE DMA FOR AN INPUT OPERATION
a. Control word 1 (CW1) is transferred to the DMA card from the A-register on the IOB lines by an OTA 6 instruction. b. Bits 0 thru 3, 13, and 15 of CW1 are stored on the DMA card. Bits 0 thru 3 specify the select code of the device involved in the data transfer. Bit 13 (if true) specifies CLC of the device after the final word is transferred. Bit 15 (if true) specifies STC of the device after each word is transferred. c. A CLC 2 instruction prepares DMA to receive control word 2 (CW2), and OTA 2 transfers CW2 to the DMA card. d. Bits 0 thru 12 and 15 of CW2 are stored on the DMA card. Bits 0 thru 12 specify the starting address in memory of the data transfer and are stored in the memory address register. Bit 15 specifies whether the transfer is a memory input or an output operation (bit 15 = logic 1 = memory input operation). e. A STC 2 instruction prepares DMA to receive control word 3 (CW3), and OTA 2 transfers CW3 to the DMA card. f. Bits 0 thru 12 of CW3 are stored in the word count register of the DMA card and specify the 2's complement of the number of words (octal) in the block length of data to be transferred. g. I/O signals turn on DMA (STC 6,C) and the I/O device (STC 10,C).
DMA DATA TRANSFER
a. Device sets interface flag when ready to transfer data, generating an SRQ signal. b. On the DMA card, an SRQ signal is compared with the stored select code of the device and, if the select code of the device that originated the SRQ signal is the same as the select code that is stored on the DMA card, a cycle request signal is originated. c. The cycle request signal causes a PH5 signal to be generated at the end of the current cycle, which: (1) Puts the computer into the phase 5 mode, disabling all other phases and the instruction register. An ISG signal inhibits the reading of memory into the T-register. (2) Disables normal I/O operation by inhibiting select code logic. (3) Reads the interface card data onto the I/O bus lines using DMA generated select code and IOI signals. (4) Gates the data from the IOB lines onto the T-bus with an IOI signal. (5) Stores the T-bus bits in the T-register using a DMA STBT signal. (6) Enables the memory address register to select the desired memory location for input. d. The computer now continues into a memory cycle. Since memory reading is inhibited, the T-register retains the input word through the read portion of the memory cycle, and the word is written into memory on the write portion of the cycle. e. At the end of the phase 5 cycle, a CLF signal and a STC signal (if selected) are issued to the interface card, releasing the device to obtain the next input word.
DATA TRANSFER COMPLETION
a. At the end of each phase 5 cycle, the memory address register and the word count register are advanced by one count. This allows the memory address register to address the next higher memory location and advances the word count register one count closer to zero from the initial negative value. b. When the word count register reaches zero, word count rollover occurs and the phase 5 cycle control is disabled. c. If the interrupt system is on, an interrupt to location 06 will occur through the interrupt system. d. Anytime during or after data transfer, the status of the word count register may be checked by LIA 2 or MIA 2 instruction, which loads the word count register into the A-register. e. A SFS 6 instruction may be used to test for transfer completion since the DMA flag is set at word count rollover. f. If selected during initialization, a CLC signal is issued to the interface card to turn off the device.

the IOB lines if the respective instruction is addressed to code 2. This allows the status of the data transfer to be checked as desired. Also, if SFC or SFS instructions are addressed to SC6 in the main program and the flag is clear or set as required by the respective instruction, a true SKF signal will result at pin 12 of the DMA card.

3-14. The last step in the initialization process consists of setting control and clearing flag FF's on the DMA card and the device interface card to or from which data is to be transferred. This is done by STC,C instructions in the program to the select code of the device and to select code 6 (the DMA select code). On the DMA card, the STC instruction sets the interrupt channel control FF and the transfer enable FF. The CLF instruction resets the flag buffer FF and flag FF. Data transfer can now begin.

3-15. GENERATION OF A PHASE 5 SIGNAL.

3-16. When the device is ready to transfer a word, an SRQ signal is generated on the appropriate SRQ line. The SRQ signal and the corresponding service select register bit are combined in a nand-gate. The resulting output is inverted by MC85B to provide the SSRQ signal. The true set output of the transfer enable FF and the SSRQ signal are combined in MC83C. The resulting false output of MC83C resets the cycle request FF at T4T5. At T7 of the same cycle, the phase 5 FF is set, generating the PH5 signal.

3-17. When the PH5 signal is generated, central processor operation is suspended for one machine cycle. To accomplish data transfer, DMA must generate control signals that would normally be generated within the central processor unit. During the phase 5 cycle, the following control signals are generated by DMA:

a. A $\overline{\text{PH5}}$ signal at pin 83 is generated by inverting the PH5 signal in MC106A. During phase 5, this signal inhibits the enable phase gate on the computer timing generator card and prevents the computer from going into phase 1, 2, 3, or 4 until phase 5 is complete.

b. An ISG signal is generated for a memory input operation by combining the PH5 and IN signals in MC105A. A true ISG signal inhibits the memory strobe time (MST) signal from being generated on the computer timing generator card.

c. IOI and $\overline{\text{SWST}}$ are generated to implement memory input operations.

d. IOCO and $\overline{\text{XRTS}}$ signals are generated to implement memory output operations.

e. An $\overline{\text{XPH4}}$ signal is generated by the update interrupt address FF during T7 which causes a phase 4 signal to be generated at the timing generator card during T7 to store M-register bits 0 through 5.

f. The $\overline{\text{PH5}}$ and CRFF signals cause MC83D to output a true signal during phase 5. This, in turn, generates an HIS

signal to the I/O control card which prevents interrupt requests from other devices from being serviced during phase 5.

3-18. DATA INPUT OPERATION.

3-19. When the phase 5 FF is set, the service select register bits are gated onto the select code lines along with the SCM1 signal. This allows DMA to address the device on the appropriate select code lines (10 through 16). At the device interface card, SCL and SCM signals from DMA are combined with an IOG signal and the resulting output is combined with an IOI signal to gate data from the interface card onto the IOB-lines.

3-20. On the DMA card, the PH5 and IN signals are combined in MC105A. The output of MC105A combines with the ENF signal to generate SWST and IOI signals. (See figure 3-2.) The IOI signal gates the IOB bits onto the T-bus in the central processor. The $\overline{\text{SWST}}$ signal is decoded by the instruction decoder in the computer. The STBT signal, which results from the $\overline{\text{SWST}}$ signal being decoded, clocks the T-bus bits into the T-register. The T-register output is then routed directly into computer memory and the data transfer for the first word is complete. This process is repeated for each word to be transferred into memory.

3-21. DATA OUTPUT OPERATION.

3-22. When the phase 5 FF is set, the service select register bits are gated onto the select code lines along with the SCM1 signal, allowing DMA to address I/O select codes 10 through 16. At the device interface card, SCL, SCM, IOG, and IOO signals from DMA are used to gate data from the IOB lines into the interface card registers. To transfer data out of computer memory and onto the IOB lines, DMA generates $\overline{\text{XRTS}}$ and IOCO control signals. (See figure 3-3.) The $\overline{\text{XRTS}}$ signal and the RTS signal from the computer instruction decoder card combine to generate the RTSB signal. The RTSB signal gates the T-register bits onto the S-bus. The S-bus bits are inverted and are gated onto the IOB lines by the IOCO signal. The IOB bits are then transferred into the interface card and the device, as mentioned previously, and a single word transfer is complete. This process is repeated until all words in the data block have been transferred.

3-23. DMA REGISTER STEPPING AND DEVICE TURN-OFF.

3-24. At T7 of phase 5, the output of MC83B goes true, and the memory address register is advanced one count by the true SMAR signal. This updates the memory address register to the memory location involved in the next word transfer. At the end of the same T7, the output of MC83A goes true and the true SWCR signal advances the word count register one count.

3-25. The above process is repeated for each phase 5 cycle until all words in the data block have been transferred. Since the word count register is initially loaded with

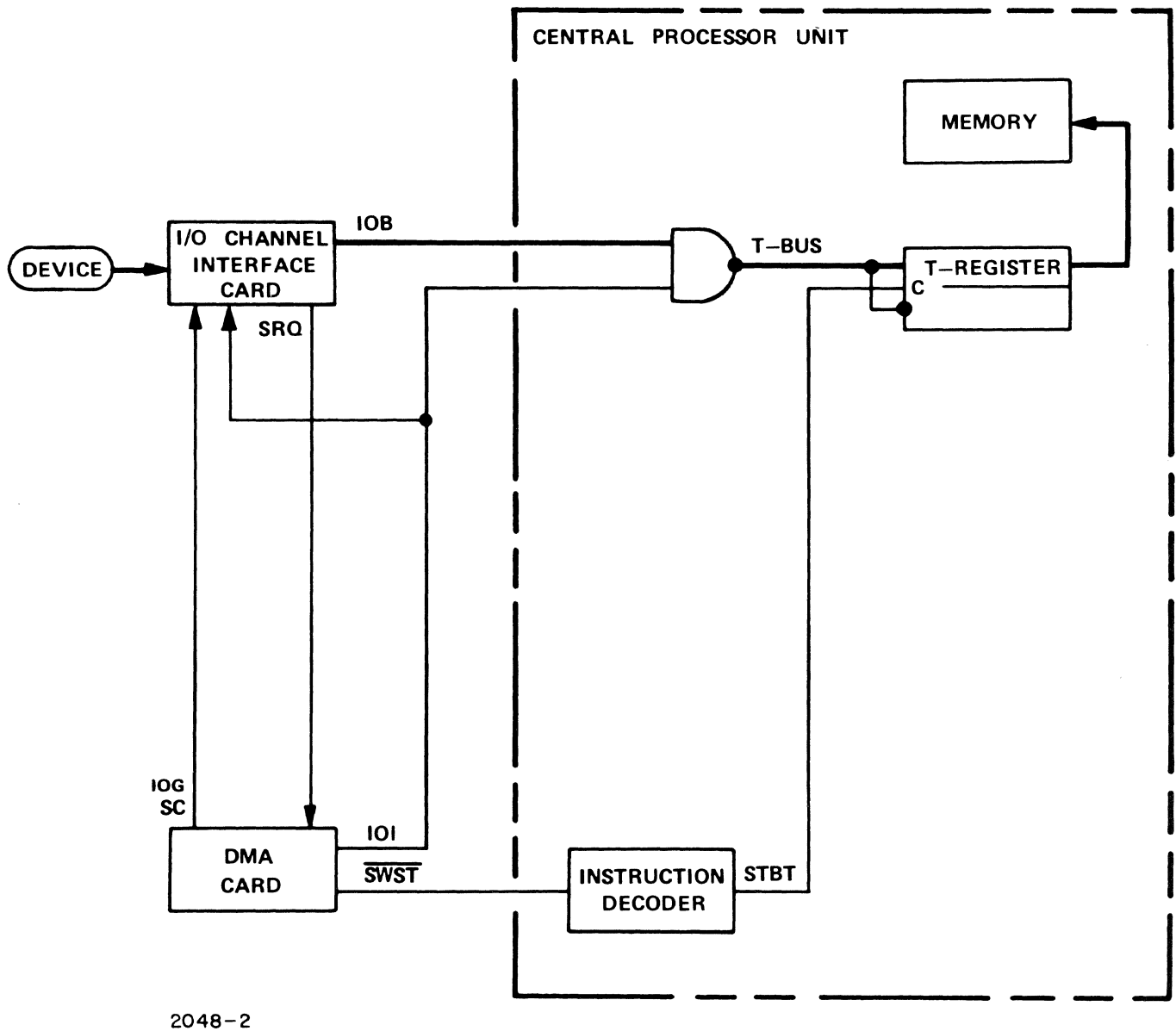
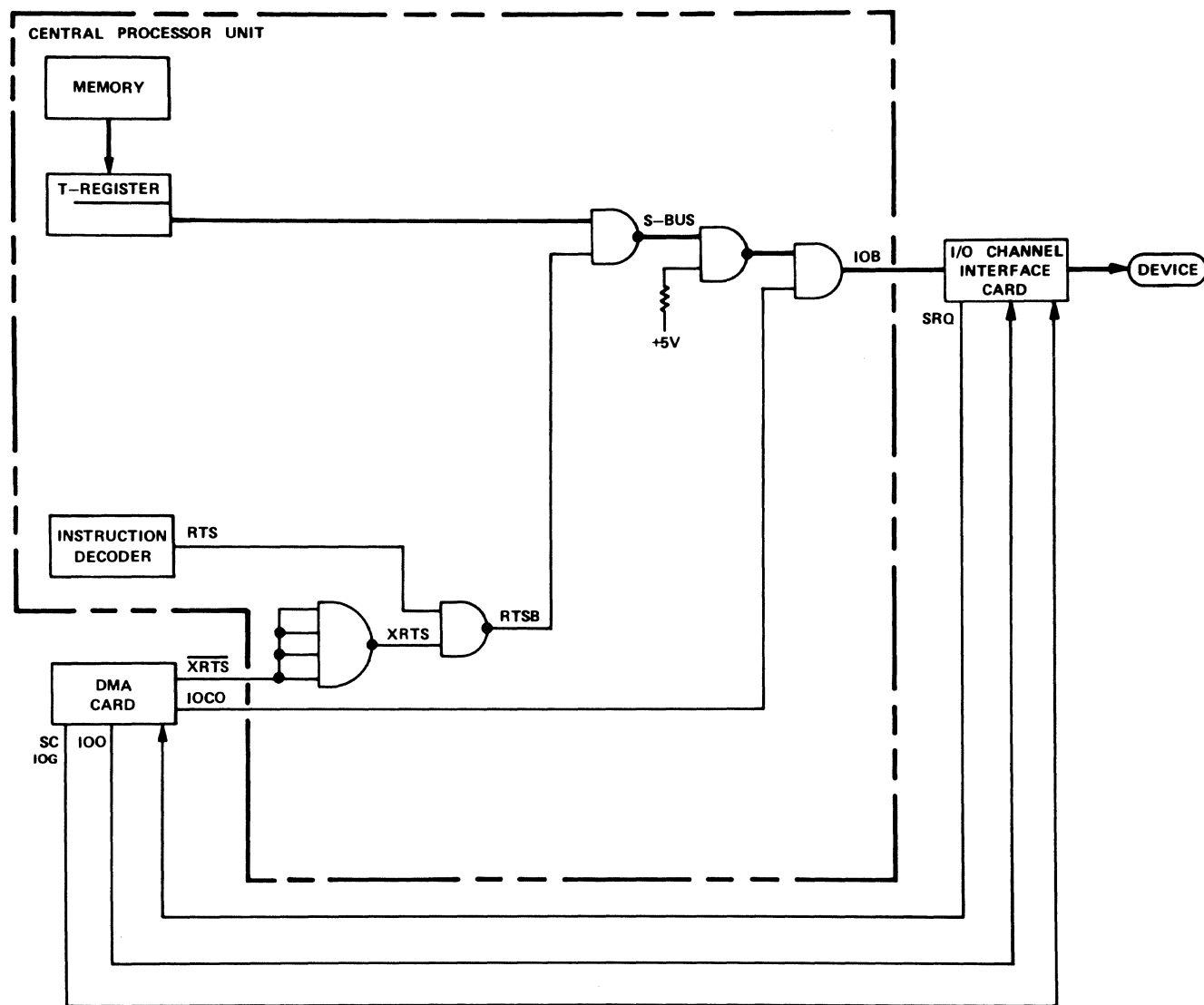


Figure 3-2. Transferring Data from an External Device to Memory



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Figure 3-3. Transferring Data from Memory to an External Device

the two's complement of the number of words in the data block, the word count register will contain all zero's when all words have been transferred. The final SWCR signal sets all WCR bits to zero and causes pin 12 of MC91 (the carry output) to go false. The false WCR signal makes the output of MC101B false, setting the flag buffer FF. At T2, the ENF signal and the true FBFF signal set the flag FF.

3-26. Setting the STC and CLC FF's during initialization causes a STC signal to be generated after each word transfer and a CLC signal to be generated after the final word transfer. The STC FF output is applied to MC101C along with the reset output of the cycle request FF and the output of MC74C. The MC74C output will be true until the last word transfer when the flag buffer FF is set. The cycle request FF is reset by every SRQ signal. Therefore, a STC signal will be generated at pin 22 of the DMA card for every word transfer except the last when the flag buffer FF is set. Also, the true output of MC74C causes a CLF signal to be generated at pin 7 every T4T5 to clear the device flag after every word transfer, except the last. The CLC FF output is applied to MC101A along with the reset output of the cycle request FF and the set output of the flag buffer FF. The false flag buffer FF output signal inhibits MC101A until after the final word transfer. The flag buffer FF signal then goes true and a CLC signal is generated at pin 21 of the DMA card to turn off the external device. This inhibits any

SRQ signals from being generated by the device until DMA is reinitialized.

3-27. DMA COMPLETION INTERRUPT.

3-28. The true FBFF and FLFF signals enable the generation of flag and interrupt signals at the end of the final word transfer. The true FLFF signal along with true ICCFF and IEN signals make MC13C output a false signal to MC37B. True signals from MC37B, FBFF, and PRH6 make MC27B output a false signal at T5 to set the interrupt request FF and generate FLG0 and IRQ6 signals. The FBFF signal also enables the generation of an EDT signal at the DMA card which is used by some of the I/O devices to signal the end of data transfer.

3-29. At the I/O control card, the FLG0 and IRQ6 signals try to generate an interrupt, but the interrupt system is disabled for at least one phase to allow a main program instruction to be executed following a phase 5 operation. At the end of this cycle, DMA interrupts, causing the generation of a phase 4 cycle and forcing the DMA trap cell location into the M-register. The next fetched instruction will be the call instruction for the DMA completion subroutine. In the DMA completion subroutine, DMA is turned off and must be reinitialized before being placed in operation again.

SECTION IV

MAINTENANCE

4-1. INTRODUCTION.

4-2. This section contains information on the diagnostics and troubleshooting for the DMA option.

4-3. DIAGNOSTICS.

4-4. Complete diagnostic procedures and listings are contained in the manual supplement attached to this manual. The manual supplement contains a DMA general diagnostic and a DMA rate and transfer diagnostic.

4-5. TROUBLESHOOTING.

4-6. Troubleshooting the DMA option is accomplished by performing the diagnostic tests contained in the manual

supplement attached to this manual and analyzing the error halts that occur as the test is being run. To further isolate trouble, refer to the list of signals and equations in table 4-1 and the DMA schematic and parts location diagrams in figure 4-1. Table 4-2 contains a list of connector pin functions for the DMA card and a listing of reference numbers for each signal. The reference numbers correspond to consecutive reference numbers on the HP 2114B Computer backplane wiring list which appears in Volume Two of the Operation and Maintenance Manual for the computer. Table 4-3 contains a complete parts list for the DMA card with parts listed in alphanumeric order of reference designations. Refer to Volumes Two and Three of the HP 2114B Operation and Maintenance Manual for additional information on backplane wiring, signal data, etc., not included in this manual.

Table 4-1. DMA Signals and Equations

MNEMONIC	SIGNAL NAME	EQUATION
CLC	Clear Control	CLC = CLC FF
CLC FF	Clear Control FF	Data = IOB13 Clock = (SC6 · IOO)
CR FF	Cycle Request FF	Data = $\overline{\text{SSRQ}} + \overline{\text{TEFF}}$ Clock = $\overline{\text{T4T5}}$
EDT	End of Data Transfer	EDT = FBFF · T4T5 · $\overline{\text{CRFF}}$
FB FF	Flag Buffer FF	Set = POPIO + (STF · SC6) + WCR Reset = (IAK · IRQFF) + (CLF · SC6)
FL FF	Flag FF	Set = FBFF · ENF Reset = CLF · SC6
FLG0	Flag 0	FLG0 = IRQFF
$\overline{\text{HIS}}$	“Not” Hold Interrupt System	$\overline{\text{HIS}}$ = $\overline{\text{PH5}} \cdot \text{CRFF}$
ICC FF	Interrupt Channel Control FF	Set = STC6 · SC6 Reset = (CLC · SC6) + (CRS + $\overline{\text{PRL4}}$)
IOCO	Input/Output Control Out	IOCO = OUT · T4T5 · PH5
IN	DMA Input	IN = IOB15 · LMAR
INI FF	Initialization Channel Control FF	Set = STC · SC2 Reset = CLC · SC2
IRQ FF	Interrupt Request FF	Set = PRH6 · T5 · IEN · FLGFF · ICCFF · FBFF Reset = ENF
IRQ6	Interrupt Request 6	IRQ6 = IRQFF
ISG	Interrupt Strobe Generator	ISG = PH5 · IN
$\overline{\text{LMAR}}$	“Not” Load Memory Address Register	$\overline{\text{LMAR}}$ = $\overline{\text{SC2}} + \overline{\text{IOO}} + \text{INIFF}$
$\overline{\text{LWCR}}$	“Not” Load Word Count Register	$\overline{\text{LWCR}}$ = $\overline{\text{SC2}} + \overline{\text{IOO}} + \text{INIFF}$
OUT	DMA Output	OUT = $\overline{\text{IN}}$
PH5	Phase 5	PH5 = PH5 FF
PH5 FF	Phase 5 FF	Data = $\overline{\text{CRFF}}$ Clock = $\overline{\text{T7}}$
PRL6	Priority Low 6	PRL6 = PRH6 · ($\overline{\text{IEN}} + \overline{\text{FLGFF}} + \overline{\text{ICCF}}$)
RWCR	Read Word Count Register	RWCR = (IOI · SC2)
SC2	Select Code 2	SC2 = IOG · SCM0 · SCL2
SC6	Select Code 6	SC6 = IOG · SCM0 · SCL6

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
SCL0	Select Code Least Significant Octal 0	$SCL0 = PH5 \cdot SS0$
SCL1	Select Code Least Significant Octal 1	$SCL1 = PH5 \cdot SS1$
SCL2	Select Code Least Significant Octal 2	$SCL2 = PH5 \cdot SS2$
SCL3	Select Code Least Significant Octal 3	$SCL3 = PH5 \cdot SS3$
SCL4	Select Code Least Significant Octal 4	$SCL4 = PH5 \cdot SS4$
SCL5	Select Code Least Significant Octal 5	$SCL5 = PH5 \cdot SS5$
SCL6	Select Code Least Significant Octal 6	$SCL6 = PH5 \cdot SS6$
SCM1	Select Code Most Significant Octal 1	$SCM1 = PH5$
SKF	Skip on Flag Signal	$SKF = (SFS \cdot SC6 \cdot FLGFF) + (SFC \cdot SC6 \cdot \overline{FLGFF})$
SMAR	Step Memory Address Register	$SMAR = PH5 \cdot T7$
SSRQ	Selected Service Request	$SSRQ = (SS0 \cdot SRQ10) +$ $(SS1 \cdot SRQ11) +$ $(SS2 \cdot SRQ12) +$ $(SS3 \cdot SRQ13) +$ $(SS4 \cdot SRQ14) +$ $(SS5 \cdot SRQ15) +$ $(SS6 \cdot SRQ16)$
STC	Set Control	$STC = STC \text{ FF}$
STC FF	Set Control FF	Data = IOB15 Clock = $(SC6 \cdot IOO) + (SC6 \cdot OUT \cdot T3T4 \cdot PH5)$
$\overline{SWCR}$	“Not” Step Word Count Register	$\overline{SWCR} = \overline{CRFF} + \overline{T7}$
$\overline{SWST}$	Switch Store in T-Register	$\overline{SWST} = \overline{ENF} + \overline{PH5} + \overline{IN}$
TE FF	Transfer Enable FF	Set = $STC \cdot SC6$ Reset = $(FLGFF \cdot T4T5) + CRS + \overline{PRL4}$
UIA FF	Update Interrupt Address FF	Set = $PH4$ Reset = $PH5 \cdot ENF$
$\overline{WCR}$	“Not” Word Count Rollover	$\overline{WCR} = WCR0 \text{ thru } WCR12 \cdot \overline{SWCR}$
WCR0	Word Count Register Bit 0	$WCR0 = WCR0 \text{ FF}$

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
WCR0 FF	Word Count Register Bit 0 FF	Clock = $\overline{\text{SWCR}}$ Direct Set = $\text{IOB0} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB0}} \cdot \text{LWCR}$
WCR1	Word Count Register Bit 1	WCR1 = WCR1 FF
WCR1 FF	Word Count Register Bit 1 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ Direct Set = $\text{IOB1} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB1}} \cdot \text{LWCR}$
WCR2	Word Count Register Bit 2	WCR2 = WCR2 FF
WCR2 FF	Word Count Register Bit 2 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}} \cdot \overline{\text{WCR1}}$ Direct Set = $\text{IOB2} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB2}} \cdot \text{LWCR}$
WCR3	Word Count Register Bit 3	WCR3 = WCR3 FF
WCR3 FF	Word Count Register Bit 3 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ thru $\overline{\text{WCR2}}$ Direct Set = $\text{IOB3} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB3}} \cdot \text{LWCR}$
WCR4	Word Count Register Bit 4	WCR4 = WCR4 FF
WCR4 FF	Word Count Register Bit 4 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ thru $\overline{\text{WCR3}}$ Direct Set = $\text{IOB4} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB4}} \cdot \text{LWCR}$
WCR5	Word Count Register Bit 5	WCR5 = WCR5 FF
WCR5 FF	Word Count Register Bit 5 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ thru $\overline{\text{WCR4}}$ Direct Set = $\text{IOB5} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB5}} \cdot \text{LWCR}$
WCR6	Word Count Register Bit 6	WCR6 = WCR6 FF
WCR6 FF	Word Count Register Bit 6 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ thru $\overline{\text{WCR5}}$ Direct Set = $\text{IOB6} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB6}} \cdot \text{LWCR}$
WCR7	Word Count Register Bit 7	WCR7 = WCR7 FF
WCR7 FF	Word Count Register Bit 7 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ thru $\overline{\text{WCR6}}$ Direct Set = $\text{IOB7} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB7}} \cdot \text{LWCR}$
WCR8	Word Count Register 8	WCR8 = WCR8 FF
WCR8 FF	Word Count Register Bit 8 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}}$ thru $\overline{\text{WCR7}}$ Direct Set = $\text{IOB8} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB8}} \cdot \text{LWCR}$

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
WCR9	Word Count Register Bit 9	WCR9 = WCR9 FF
WCR9 FF	Word Count Register Bit 9 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}} \text{ thru } \overline{\text{WCR8}}$ Direct Set = $\text{IOB9} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB9}} \cdot \text{LWCR}$
WCR10	Word Count Register Bit 10	WCR10 = WCR10 FF
WCR10 FF	Word Count Register Bit 10 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}} \text{ thru } \overline{\text{WCR9}}$ Direct Set = $\text{IOB10} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB10}} \cdot \text{LWCR}$
WCR11	Word Count Register Bit 11	WCR11 = WCR11 FF
WCR11 FF	Word Count Register Bit 11 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}} \text{ thru } \overline{\text{WCR10}}$ Direct Set = $\text{IOB11} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB11}} \cdot \text{LWCR}$
WCR12	Word Count Register Bit 12	WCR12 = WCR12 FF
WCR12 FF	Word Count Register Bit 12 FF	Clock = $\overline{\text{SWCR}} \cdot \overline{\text{WCR0}} \text{ thru } \overline{\text{WCR11}}$ Direct Set = $\text{IOB12} \cdot \text{LWCR}$ Direct Reset = $\overline{\text{IOB12}} \cdot \text{LWCR}$
XMR0	External M-Register Bit 0	XMR0 = XMR0 FF
XMR0 FF	External M-Register Bit 0 FF	Clock = SMAR Direct Set = $\text{IOB0} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB0}} \cdot \text{LMAR}$
XMR1	External M-Register Bit 1	XMR1 = XMR1 FF
XMR1 FF	External M-Register Bit 1 FF	Clock = $\text{SMAR} \cdot \overline{\text{XMR0}}$ Direct Set = $\text{IOB} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB}} \cdot \text{LMAR}$
XMR2	External M-Register Bit 2	XMR2 = XMR2 FF
XMR2 FF	External M-Register Bit 2 FF	Clock = $\text{SMAR} \cdot \overline{\text{XMR0}} \cdot \overline{\text{XMR1}}$ Direct Set = $\text{IOB2} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB2}} \cdot \text{LMAR}$
XMR3	External M-Register Bit 3	XMR3 = XMR3 FF
XMR3 FF	External M-Register Bit 3 FF	Clock = $\text{SMAR} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR2}}$ Direct Set = $\text{IOB3} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB3}} \cdot \text{LMAR}$
XMR4	External M-Register Bit 4	XMR4 = XMR4 FF

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
XMR4 FF	External M-Register Bit 4 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR3}}$ Direct Set = $\text{IOB4} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB4}} \cdot \text{LMAR}$
XMR5	External M-Register Bit 5	XMR5 = XMR5 FF
XMR5 FF	External M-Register Bit 5 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR4}}$ Direct Set = $\text{IOB5} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB5}} \cdot \text{LMAR}$
XMR6	External M-Register Bit 6	XMR6 = XMR6 FF
XMR6 FF	External M-Register Bit 6 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR5}}$ Direct Set = $\text{IOB6} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB6}} \cdot \text{LMAR}$
XMR7	External M-Register Bit 7	XMR7 = XMR7 FF
XMR7 FF	External M-Register Bit 7 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR6}}$ Direct Set = $\text{IOB7} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB7}} \cdot \text{LMAR}$
XMR8	External M-Register Bit 8	XMR8 = XMR8 FF
XMR8 FF	External M-Register Bit 8 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR7}}$ Direct Set = $\text{IOB8} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB8}} \cdot \text{LMAR}$
XMR9	External M-Register Bit 9	XMR9 = XMR9 FF
XMR9 FF	External M-Register Bit 9 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR8}}$ Direct Set = $\text{IOB9} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB9}} \cdot \text{LMAR}$
XMR10	External M-Register Bit 10	XMR10 = XMR10 FF
XMR10 FF	External M-Register Bit 10 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR9}}$ Direct Set = $\text{IOB10} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB10}} \cdot \text{LMAR}$
XMR11	External M-Register Bit 11	XMR11 = XMR11 FF
XMR11 FF	External M-Register Bit 11 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR10}}$ Direct Set = $\text{IOB11} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB11}} \cdot \text{LMAR}$
XMR12	External M-Register Bit 12	XMR12 = XMR12 FF
XMR12 FF	External M-Register Bit 12 FF	Clock = $\overline{\text{SMAR}} \cdot \overline{\text{XMR0}} \text{ thru } \overline{\text{XMR11}}$ Direct Set = $\text{IOB12} \cdot \text{LMAR}$ Direct Reset = $\overline{\text{IOB12}} \cdot \text{LMAR}$

Table 4-1. DMA Signals and Equations (Continued)

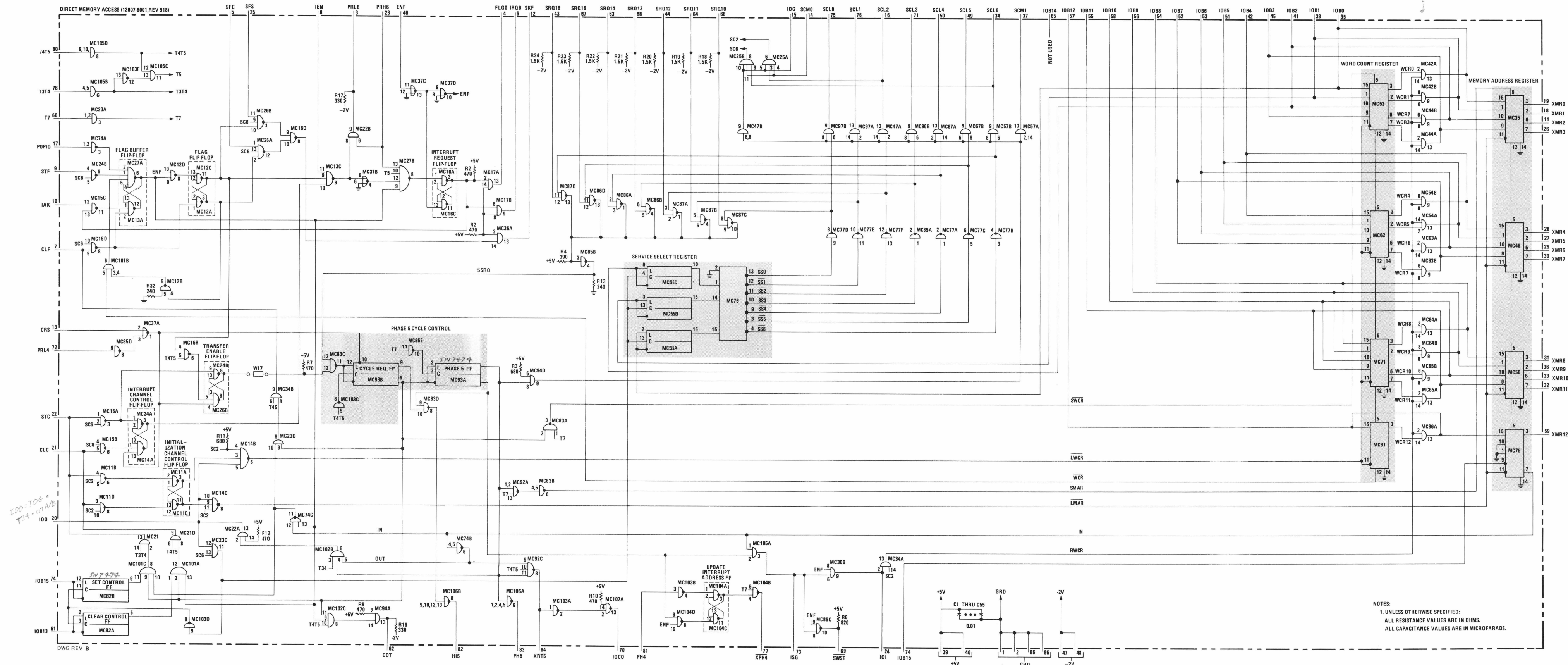
MNEMONIC	SIGNAL NAME	EQUATION
XPH4	External Phase 4	$XPH4 = \overline{T7} + \overline{UIA} FF$
$\overline{XRTS}$	"Not" External Read T to S-Bus	$\overline{XRTS} = \overline{OUT} + \overline{T4T5} + \overline{PH5}$

Table 4-2. Connector Pin Index

PIN	FUNCTION	REF	PIN	FUNCTION	REF
1	Ground	337	44	SRQ12	327
2	Ground	337	45	IOB3	109
3	PRL6	334	46	ENF	067
4	FLG0	323	47	-2 volts	336
5	SFC	010	48	-2 volts	336
6	IRQ6	240	49	SCL5	225
7	CLF	013	50	SCL4	224
8	IEN	233	51	IOB5	133
9	STF	006	52	IOB7	135
10	IAK	232	53	IOB6	134
11	XMR2	514	54	IOB8	156
12	SKF	252	55	IOB11	159
13	CRS	234	56	IOB9	157
14	SCM0	228	57	IOB12	178
15	IOG	038	58	IOB10	158
16	SCL2	222	59	XMR12	524
17	POPIO	078	60	T7	093
18	XMR1	513	61	IOB13	179
19	XMR0	512	62	EDT	526
20	IOO	020	63	SRQ14	329
21	CLC	014	64	SRQ11	326
22	STC	011	65	IOB14	180
23	PRH6	258	66	SRQ10	325
24	IOI	019	67	SRQ15	330
25	SFS	012	68	SRQ13	328
26	XMR3	515	69	SWST	083
27	XMR5	517	70	IOCO	027
28	XMR4	516	71	SCL3	223
29	XMR6	518	72	PRL4	255
30	XMR7	519	73	ISG	315
31	XMR8	520	74	IOB15	181
32	XMR11	523	75	SCL0	220
33	XMR10	522	76	SCL1	221
34	SCL6	226	77	XPH4	310
35	IOB0	106	78	T3T4	097
36	XMR9	521	79	Not used	—
37	SCM1	227	80	T4T5	098
38	IOB1	107	81	PH4	076
39	+5 volts	335	82	HIS	312
40	+5 volts	335	83	PH5	313
41	IOB2	108	84	XRTS	525
42	IOB4	132	85	Ground	338
43	SRQ16	331	86	Ground	338

Table 4-3. DMA Card Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR. CODE NO.	MFR. PART NO.
C1 thru C55	0160-2055	C: FXD CER 0.01 UF +80-20% 100 VDCW	91418	TA
MC11,12,15,16,24,74,83,104	1820-0054	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7400N
MC13,14,26, 92	1820-0068	INTEGRATED CIRCUIT: TTL	56289	USN7410A
MC17,21,22,34,36,42,44,47,54, 57,63 thru 67,94, 96,97,107	1820-0956	INTEGRATED CIRCUIT: CTL	07263	SL3459
MC23,105	1820-0141	INTEGRATED CIRCUIT	28480	1820-0141
MC25,101,102	1820-0372	INTEGRATED CIRCUIT: TTL	01295	SN74H11N
MC27	1820-0069	INTEGRATED CIRCUIT: TTL	56289	USN7420A
MC35,46,53,56,62,71,75,91	1820-0233	INTEGRATED CIRCUIT: TTL	01295	SN10625
MC37	1820-0328	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7402N
MC55	1820-0301	INTEGRATED CIRCUIT: QUAD BISTABLE LATCH	01285	SN7475N
MC82,93	1820-0077	INTEGRATED CIRCUIT: "D" EDGE TRANSFER FLIP-FLOP	01295	SN7474N
MC85,103	1820-0132	INTEGRATED CIRCUIT: TTL	07263	U6A901659X
MC86,87	1820-0327	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7401N
MC106	1820-0071	INTEGRATED CIRCUIT: 4-INPUT DR NAND	01295	SN7440N
R1	0683-1015	R: FXD COMP 100 OHM 5% 1/4W	01121	CB 1015
R2,7,9,10,12	0683-4715	R: FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
R3,11	0683-6815	R: FXD COMP 680 OHM 5% 1/4W	01121	CB 6815
R4	0683-3915	R: FXD COMP 390 OHM 5% 1/4W	01121	CB 3915
R5,16,17	0683-3315	R: FXD COMP 330 OHM 5% 1/4W	01121	CB 3315
R6	0683-8215	R: FXD COMP 820 OHM 5% 1/4W	01121	CB 8215
R13,32	0683-2415	R: FXD COMP 240 OHM 5% 1/4W	01121	CB 2415
R18 thru R24	0683-1525	R: FXD COMP 1500 OHM 5% 1/4W	01121	CB 1525
W1	8159-0005	JUMPER WIRE	28480	8159-0005



4-9/4-10

SECTION V

REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the DMA option. Table 5-1 lists parts in alphanumeric order of the HP stock numbers and lists the following information on each part:

a. Description of the part. (Refer to table 5-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 5-3.

c. Manufacturer's part number.

d. Total quantity of each part used in the DMA option.

5-3. A separate parts list is provided along with the parts location diagram for the DMA card in section IV of this manual. This parts list lists the parts in alphanumeric order of reference designation.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Instrument model and serial number.

b. Hewlett-Packard stock number for each part.

c. Description of each part.

d. Circuit reference designation.

Table 5-1. Replaceable Parts

HP PART NO.	DESCRIPTION	MFR	MFR PART NO.	TQ
0160-2055	C:FXD CER 0.01 UF +80-20% 100VDCW	91428	TA	55
0683-1015	R:FXD COMP 100 OHM 5% 1/4W	01121	CB 1015	1
0683-1525	R:FXD COMP 1500 OHM 5% 1/4W	01121	CB 1525	7
0683-2415	R:FXD COMP 240 OHM 5% 1/4W	01121	CB 2415	2
0683-3315	R:FXD COMP 330 OHM 5% 1/4W	01121	CB 3315	3
0683-3915	R:FXD COMP 390 OHM 5% 1/4W	01121	CB 3915	1
0683-4715	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715	5
0683-6815	R:FXD COMP 680 OHM 5% 1/4W	01121	CB 6815	2
0683-8215	R:FXD COMP 820 OHM 5% 1/4W	01121	CB 8215	1
1820-0054	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7400N	8
1820-0068	INTEGRATED CIRCUIT: TTL	56289	USN7410A	4
1820-0069	INTEGRATED CIRCUIT: TTL	56289	USN7420A	1
1820-0071	INTEGRATED CIRCUIT: 4-INPUT DR NAND	01295	SN7440N	1
1820-0077	INTEGRATED CIRCUIT: "D" EDGE TRIGGER F/F	01295	SN7474N	2
1820-0132	INTEGRATED CIRCUIT: TTL	07263	U6A901659X	2
1820-0141	INTEGRATED CIRCUIT	28480	1820-0141	2
1820-0233	INTEGRATED CIRCUIT: TTL	01295	SN10625	8
1820-0301	INTEGRATED CIRCUIT: QUAD BISTABLE LATCH	01295	SN7475N	1
1820-0327	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7401N	2
1820-0328	INTEGRATED CIRCUIT: QUAD 2-INPUT NOR	01295	SN7402N	1
1820-0372	INTEGRATED CIRCUIT: TTL	01295	SN74H11N	3
1820-0956	INTEGRATED CIRCUIT: CTL	07263	SL3459	18
8159-0005	JUMPER WIRE	28480	8159-0005	1
12607-6001	DIRECT MEMORY ACCESS KIT	28480	12607-6001	1

Table 5-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS		
A = assembly	J = receptacle connector	TB = terminal board
B = motor	K = relay	TP = test point
BT = battery	L = inductor	U = integrated circuit
C = capacitor	M = meter	V = vacuum tube, neon bulb, photocell, etc.
CP = coupler	MC = microcircuit	VR = voltage regulator
CR = diode	P = plug connector	W = cable, jumper
DL = delay line	Q = transistor	X = socket
DS = device signaling (lamp)	R = resistor	Y = crystal
E = misc hardware	RT = thermistor	Z = tuned cavity, network
F = fuse	S = switch	
FL = filter	T = transformer	

ABBREVIATIONS		
A = amperes	IMPG = impregnated	P/O = part of
AC = alternating current	IN. = inch, inches	POLY = polystyrene
AFC = automatic frequency control	INCD = incandescent	PORC = porcelain
ALUM = aluminum	INCL = include(s)	POS = position(s)
AL-ELECT = aluminum electrolytic	INS = insulation(ed)	POT = potentiometer
ASSY = assembly	INT = internal	PP = peak-to-peak
BFO = beat frequency oscillator	I/O = input/output	PT = point
BE CU = beryllium copper	K = kilo = 1000	PWV = peak working voltage
BH = binder head	LH = left hand	R = resistor
BP = bandpass	LIN = linear taper	RECT = rectifier
BRS = brass	LK WASH = lock washer	RF = radio frequency
BWO = backward wave oscillator	LOG = logarithmic taper	RH = round head or right hand
C = capacitor	LPF = low pass filter	RMO = rack mount only
CCW = counterclockwise	M = milli = 10^{-3}	RMS = root-mean square
CER = ceramic	MEG = mega = 10^6	RWV = reverse working voltage
CMO = cabinet mount only	MET FLM = metal film	S-B = slow-blow
COEF = coefficient	MET OX = metal oxide	SCR = screw
COM = common	MFR = manufacturer	SE = selenium
COMP = composition	MHz = megahertz	SECT = section(s)
COMPL = complete	MINAT = miniature	SEMICON = semiconductor
CONN = connector	MOM = momentary	SI = silicon
CP = cadmium plate	MTG = mounting	SIL = silver
CRT = cathode-ray tube	MY = Mylar	SL = slide
CTL = capacitor-transistor logic	N = nano (10^{-9})	SPDT = single-pole, double-throw
CW = clockwise	N/C = normally closed	SPG = spring
DC = direct current	NE = neon	SPL = special
DEPC = deposited carbon	NI PL = nickel plate	SPST = single-pole, single-throw
DPDT = double-pole, double-throw	NO. = number	SR = split ring
DPST = double-pole, single-throw	N/O = normally open	SST = stainless steel
DR = drive	NPN = negative-positive-negative	STL = steel
ELECT = electrolytic	NPO = negative positive zero (zero temperature coefficient)	TA = tantalum
ENCAP = encapsulated	NRFR = not recommended for field replacement	TD = time delay
EXT = external	NSR = not separately replaceable	TGL = toggle
F = farads	OBD = order by description	THD = thread
FH = flat head	OD = outer diameter	TI = titanium
FIL H = fillister head	OH = oval head	TOL = tolerance
FXD = fixed	OX = oxide	TRIM = trimmer
G = giga (10^9)	P = peak	TTL = transistor-transistor logic
GE = germanium	PC = printed circuit	TWT = traveling wave tube
GL = glass	PF = picofarads = 10^{-12} farads	U (μ) = micro = 10^{-6}
GND/GRD = ground(ed)	PH = Phillips head	VAR = variable
H = henries	PH BRZ = phosphor bronze	VDCW = direct current working volts
HDW = hardware	PHL = Phillips	W/ = with
HEX = hexagonal	PIV = peak inverse voltage	W = watts
HG = mercury	PNP = positive-negative-positive	WIV = working inverse voltage
HR = hour(s)		WW = wirewound
HZ = hertz		W/O = without
ID = inner diameter		
IF = intermediate frequency		

Table 5-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) and their latest supplements. The date of revision and the date of the supplements used appear at the bottom of each page. Alphabetical codes have been arbitrarily assigned to suppliers not appearing in the H4 Handbooks.

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
00000	U. S. A. Common	Any supplier of U. S.	05245	Components Corp.	Chicago, Ill.	09145	Tech. Ind. Inc. Atohm Elect.	Burbank, Calif.
00136	McCoy Electronics	Mount Holly Springs, Pa.	05277	Westinghouse Electric Corp.		09250	Electro Assemblies, Inc.	Chicago, Ill.
00213	Sage Electronics Corp.	Rochester, N. Y.		Semi-Conductor Dept.	Youngwood, Pa.	09353	C & K Components Inc.	Newton, Mass.
00287	Cemco Inc.	Danielson, Conn.	05347	Ultronix, Inc.	San Mateo, Calif.	09569	Mallory Battery Co. of	
00334	Humidial	Colton, Calif.	05397	Union Carbide Corp., Elect. Div.			Canada, Ltd.	Toronto, Ontario, Canada
00348	Microtron Co., Inc.	Valley Stream, N. Y.			New York, N. Y.	09922	Burdry Corp.	Norwalk, Conn.
00373	Garlock Inc.	Cherry Hill, N. J.	05574	Viking Ind. Inc.	Canoga Park, Calif.	10214	General Transistor Western Corp.	
00656	Aerovox Corp.	New Bedford, Mass.	05593	Icore Electro-Plastics Inc.	Sunnyvale, Calif.			Los Angeles, Calif.
00779	Amp. Inc.	Harrisburg, Pa.	05616	Cosmo Plastic		10411	Ti-Tal, Inc.	Berkeley, Calif.
00781	Aircraft Radio Corp.	Boonton, N. J.		(c-o Electrical Spec. Co.)	Cleveland, Ohio	10646	Carborundum Co.	Niagara Falls, N. Y.
00815	Northern Engineering Laboratories, Inc.	Burlington, Wis.	05624	Barber Colman Co.	Rockford, Ill.	11236	CTS of Berne, Inc.	Berne, Ind.
			05728	Tiffen Optical Co.		11237	Chicago Telephone of California, Inc.	
00853	Sangamo Electric Co., Pickens Div.			Roslyn Heights, Long Island, N. Y.				So. Pasadena, Calif.
		Pickens, S. C.	05729	Metro-Tel Corp.	Westbury, N. Y.	11242	Bay State Electronics Corp.	Waltham, Mass.
00866	Goe Engineering Co.	City of Industry, Cal.	05783	Stewart Engineering Co.	Santa Cruz, Calif.	11312	Teledyne Inc., Microwave Div.	Palo Alto, Calif.
00891	Carl E. Holmes Corp.	Los Angeles, Calif.	05820	Wakefield Engineering Inc.	Wakefield, Mass.	11314	National Seal	Downey, Calif.
00929	Microfab Inc.	Livingston, N. J.	06004	Bassick Co., Div. of Stewart Warner Corp.		11453	Precision Connector Corp.	Jamaica, N. Y.
01002	General Electric Co., Capacitor Dept.				Bridgeport, Conn.	11534	Duncan Electronics Inc.	Costa Mesa, Calif.
		Hudson Falls, N. Y.	06090	Raychem Corp.	Redwood City, Calif.	11711	General Instrument Corp., Semiconductor	
01009	Alden Products Co.	Brockton, Mass.	06175	Bausch and Lomb Optical Co.	Rochester, N. Y.		Div., Products Group	Newark, N. J.
01121	Allen Bradley Co.	Milwaukee, Wis.	06402	E. T. A. Products Co. of America	Chicago, Ill.	11717	Imperial Electronic, Inc.	Buena Park, Calif.
01255	Litton Industries, Inc.	Beverly Hills, Calif.	06540	Amatom Electronic Hardware Co., Inc.		11870	Melabs, Inc.	Palo Alto, Calif.
01281	TRW Semiconductors, Inc.	Lawndale, Calif.			New Rochelle, N. Y.	12040	National Semiconductor	Danbury, Conn.
01295	Texas Instruments, Inc.,		06555	Beede Electrical Instrument Co., Inc.		12136	Philadelphia Handle Co.	Camden, N. J.
	Transistor Products Div.	Dallas, Texas	06666	General Devices Co., Inc.		12361	Grove Mfg. Co., Inc.	Shady Grove, Pa.
01349	The Alliance Mfg. Co.	Alliance, Ohio	06751	Components Inc., Ariz. Div.	Phoenix, Ariz.	12574	Gulton Ind. Inc. Data System Div.	
01589	Pacific Relays, Inc.	Van Nuys, Calif.	06812	Torrington Mfg. Co., West Div.				Albuquerque, N. M.
01670	Gudebrod Bros. Silk Co.	New York, N. Y.			Van Nuys, Calif.	12697	Clarostat Mfg. Co.	Dover, N. H.
01930	Amerock Corp.	Rockford, Ill.	06980	Varian Assoc. Eimac Div.	San Carlos, Calif.	12728	Elmar Filter Corp.	W. Haven, Conn.
01961	Pulse Engineering Co.	Santa Clara, Calif.	07088	Kelvin Electric Co.	Van Nuys, Calif.	12859	Nippon Electric Co., Ltd.	Tokyo, Japan
02114	Ferroxcube Corp. of America	Saugerties, N. Y.	07126	Digitran Co.	Pasadena, Calif.	12881	Metex Electronics Corp.	Clark, N. J.
02116	Wheelock Signals, Inc.	Long Branch, N. J.	07137	Transistor Electronics Corp.	Minneapolis, Minn.	12930	Delta Semiconductor Inc.	Newport Beach, Calif.
02286	Cole Rubber and Plastics Inc.	Sunnyvale, Calif.	07138	Westinghouse Electric Corp.		12954	Dickson Electronics Corp.	Scottsdale, Arizona
02660	Amphenol-Borg Electronics Corp.	Broadview, Ill.		Electronic Tube Div.	Elmira, N. Y.	13103	Thermolloy	Dallas, Texas
02735	Radio Corp. of America, Semiconductor		07149	Filmohm Corp.	New York, N. Y.	13396	Telefunken (GmbH)	Hanover, Germany
	and Materials Div.	Somerville, N. J.	07233	Cinch-Graphik Co.	City of Industry, Calif.	13835	Midland-Wright Div. of Pacific Industries, Inc.	
02771	Vocaline Co. of America, Inc.		07256	Silicon Transistor Corp.	Carle Place, N. Y.			Kansas City, Kansas
		Old Saybrook, Conn.	07261	Avnet Corp.	Culver City, Calif.	14099	Sem-Tech	Newbury Park, Calif.
02777	Hopkins Engineering Co.	San Fernando, Calif.	07263	Fairchild Camera & Inst. Corp.		14193	Calif. Resistor Corp.	Santa Monica, Calif.
02875	Hudson Tool & Die Co.	Newark, N. J.		Semiconductor Div.	Mountain View, Calif.	14298	American Components, Inc.	Conshohocken, Pa.
03058	G. E. Semiconductor Prod. Dept.	Syracuse, N. Y.	07322	Minnesota Rubber Co.	Minneapolis, Minn.	14433	ITT Semiconductor, A Div. of Int. Telephone	
03705	Apex Machine & Tool Co.	Dayton, Ohio	07387	Birtcher Corp., The	Monterey Park, Calif.		& Telegraph Corp.	West Palm Beach, Fla.
03797	Eldema Corp.	Compton, Calif.	07397	Sylvania Elect. Prod. Inc., Mt. View Operations	Mountain View, Calif.	14493	Hewlett-Packard Company	Loveland, Colo.
03818	Parker Seal Co.	Los Angeles, Calif.	07700	Technical Wire Products Inc.	Cranford, N. J.	14655	Cornell Dublier Electric Corp.	Newark, N. J.
03877	Transitron Electric Corp.	Wakefield, Mass.	07829	Bodine Elect. Co.	Chicago, Ill.	14674	Corning Glass Works	Corning, N. Y.
03888	Pyrofilm Resistor Co., Inc.	Cedar Knolls, N. J.	07910	Continental Device Corp.	Hawthorne, Calif.	14752	Electro Cube Inc.	San Gabriel, Calif.
03954	Singer Co., Diehl Div.		07933	Raytheon Mfg. Co.,		14960	Williams Mfg. Co.	San Jose, Calif.
	Finderne Plant	Sumerville, N. J.		Semiconductor Div.	Mountain View, Calif.	15203	Webster Electronics Co.	New York, N. Y.
04009	Arrow, Hart and Hegeman Elect. Co.		07980	Hewlett-Packard Co., Boonton Radio Div.		15287	Scionics Corp.	Northridge, Calif.
		Hartford, Conn.			Rockaway, N. J.	15291	Adjustable Bushing Co.	N. Hollywood, Calif.
04013	Taurus Corp.	Lambertville, N. J.				15558	Micron Electronics	
04062	Arco Electronic Inc.	Great Neck, N. Y.	08145	U. S. Engineering Co.	Los Angeles, Calif.			Garden City, Long Island, N. Y.
04222	Hi-Q Division of Aerovox	Myrtle Beach, S. C.	08289	Blinn, Delbert Co.	Pomona, Calif.	15566	Amprobe Inst. Corp.	Lynbrook, N. Y.
04354	Precision Paper Tube Co.	Wheeling, Ill.	08358	Burgess Battery Co.		15631	Cabletronics	Costa Mesa, Calif.
04404	Dymec Division of Hewlett-Packard Co.				Niagara Falls, Ontario, Canada	15772	Twentieth Century Coil Spring Co.	
		Palo Alto, Calif.	08524	Deutsch Fastener Corp.	Los Angeles, Calif.			Santa Clara, Calif.
04651	Sylvania Electric Products, Microwave		08664	Bristol Co., The	Waterbury, Conn.	15801	Fenwal Elect. Inc.	Framingham, Mass.
	Device Div.	Mountain View, Calif.	08717	Sloan Company	Sun Valley, Calif.	15818	Amelco Inc.	Mt. View, Calif.
04673	Dakota Engr. Inc.	Culver City, Calif.	08718	ITT Cannon Electric Inc., Phoenix Div.		16037	Spruce Pine Mica Co.	Spruce Pine, N. C.
04713	Motorola, Inc., Semiconductor Prod. Div.				Phoenix, Arizona	16179	Omni-Spectra Inc.	Farmington, Mich.
		Phoenix, Arizona	08727	National Radio Lab. Inc.	Paramus, N. J.	16352	Computer Diode Corp.	Lodi, N. J.
04732	Filtron Co., Inc. Western Div.		08792	CBS Electronics Semiconductor		16585	Boots Aircraft Nut Corp.	Pasadena, Calif.
		Culver City, Calif.		Operations, Div of C. B. S. Inc.		16688	Ideal Prec. Meter Co., Inc.	
04773	Automatic Electric Co.	Northlake, Ill.			Lowell, Mass.		De Jur Meter Div.	Brooklyn, N. Y.
04796	Sequoia Wire Co.	Redwood City, Calif.	08806	General Electric Co. Miniat. Lamp Dept.		16758	Delco Radio Div. of G. M. Corp.	Kokoma, Ind.
04811	Precision Coil Spring Co.	El Monte, Calif.			Cleveland, Ohio	17109	Thermonics Inc.	Canoga Park, Calif.
04870	P. M. Motor Company	Westchester, Ill.	08984	Mel-Rain	Indianapolis, Ind.	17474	Tranex Company	Mountain View, Calif.
04919	Component Mfg. Service Co.		09026	Babcock Relays Div.	Costa Mesa, Calif.	17554	Components Inc.	Biddeford, Me.
		W. Bridgewater, Mass.	09134	Texas Capacitor Co.	Houston, Texas	17675	Hamlin Metal Products Corp.	Akron, Ohio
05006	Twentieth Century Plastics, Inc.					17745	Angstrom Prec. Inc.	No. Hollywood, Calif.
		Los Angeles, Calif.						

Table 5-3. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
17870	McGraw-Edison Co.	Manchester, N. H.	62119	Universal Electric Co.	Owosso, Mich.	73899	JFD Electronics Corp.	Brooklyn, N. Y.
18042	Power Design Pacific Inc.	Palo Alto, Calif.	63743	Ward-Leonard Electric Co.	Mt. Vernon, N. Y.	73905	Jennings Radio Mfg. Corp.	San Jose, Calif.
18083	Clevite Corp., Semiconductor Div.	Palo Alto, Calif.	64959	Western Electric Co., Inc.	New York, N. Y.	73957	Groov-Pin Corp.	Ridgefield, N. J.
18324	Signetics Corp.	Sunnyvale, Calif.	65092	Weston Inst. Inc. Weston-Newark	Newark, N. J.	74276	Signalite Inc.	Neptune, N. J.
18476	Ty-Car Mfg. Co., Inc.	Holliston, Mass.	66295	Witteck Mfg. Co.	Chicago, Ill.	74455	J. H. Winns, and Sons	Winchester, Mass.
18486	TRW Elect. Comp. Div.	Des Plaines, Ill.	66346	Minnesota Mining & Mfg. Co. Revere Mincom Div.	St. Paul, Minn.	74861	Industrial Condenser Corp.	Chicago, Ill.
18583	Curtis Instrument, Inc.	Mt. Kisco, N. Y.	70276	Allen Mfg. Co.	Hartford, Conn.	74868	R. F. Products Division of Amphenol-Borg Electronics Corp.	Danbury, Conn.
18612	Vishay Instruments Inc.	Malvern, Pa.	70309	Allied Control	New York, N. Y.	74970	E. F. Johnson Co.	Waseca, Minn.
18873	E. I. DuPont and Co., Inc.	Wilmington, Del.	70318	Allmetal Screw Product Co., Inc.	Garden City, N. Y.	75042	International Resistance Co.	Philadelphia, Pa.
18911	Durant Mfg. Co.	Milwaukee, Wis.	70417	Amplex, Div. of Chrysler Corp.	Detroit, Mich.	75263	Keystone Carbon Co., Inc.	St. Marys, Pa.
19315	The Bendix Corp., Navigation & Control Div.	Teterboro, N. J.	70485	Atlantic India Rubber Works, Inc.	Chicago, Ill.	75378	CTS Knights Inc.	Sandwich, Ill.
19500	Thomas A. Edison Industries, Div. of McGraw-Edison Co.	West Orange, N. J.	70563	Amperite Co., Inc.	Union City, N. J.	75382	Kulka Electric Corporation	Mt. Vernon, N. Y.
19589	Concoa	Baldwin Park, Calif.	70674	ADC Products Inc.	Minneapolis, Minn.	75818	Lenz Electric Mfg. Co.	Chicago, Ill.
19644	LRC Electronics	Horseheads, N. Y.	70903	Belden Mfg. Co.	Chicago, Ill.	75915	Littlefuse, Inc.	Des Plaines, Ill.
19701	Electra Mfg. Co.	Independence, Kansas	70998	Bird Electronic Corp.	Cleveland, Ohio	76005	Lord Mfg. Co.	Erie, Pa.
20183	General Atomics Corp.	Philadelphia, Pa.	71002	Birnbach Radio Co.	New York, N. Y.	76210	C. W. Marwedel	San Francisco, Calif.
21226	Executone, Inc.	Long Island City, N. Y.	71034	Bliley Electric Co., Inc.	Erie, Pa.	76433	General Instrument Corp., Micamold Division	Newark, N. J.
21335	Fafnir Bearing Co., The	New Britain, Conn.	71041	Boston Gear Works Div. of Murray Co. of Texas	Quincy, Mass.	76487	James Millen Mfg. Co., Inc.	Malden, Mass.
21520	Fansteel Metallurgical Corp.	N. Chicago, Ill.	71218	Bud Radio, Inc.	Willoughby, Ohio	76493	J. W. Miller Co.	Los Angeles, Calif.
23042	Texscan Corp.	Indianapolis, Ind.	71279	Cambridge Thermionics Corp.	Cambridge, Mass.	76530	Cinch-Monadnock, Div. of United Carr Fastener Corp.	San Leandro, Calif.
23783	British Radio Electronics Ltd.	Washington, D. C.	71286	Camloc Fastener Corp.	Paramus, N. J.	76545	Mueller Electric Co.	Cleveland, Ohio
24455	G. E. Lamp Division	Nela Park, Cleveland, Ohio	71313	Cardwell Condenser Corp.	Lindenhurst L. I., N. Y.	76703	National Union	Newark, N. J.
24655	General Radio Co.	West Concord, Mass.	71400	Bussmann Mfg. Div. of McGraw-Edison Co.	St. Louis, Mo.	76854	Oak Manufacturing Co.	Crystal Lake, Ill.
24681	Memcor Inc., Comp. Div.	Huntington, Ind.	71436	Chicago Condenser Corp.	Chicago, Ill.	77058	The Bendix Corp., Electrodynamics Div.	N. Hollywood, Calif.
24796	Pareico Inc.	San Juan Capistrano, Calif.	71447	Calif. Spring Co., Inc.	Pico-Rivera, Calif.	77075	Pacific Metals Co.	San Francisco, Calif.
26365	Gries Reproducer Corp.	New Rochelle, N. Y.	71450	CTS Corp.	Elkhart, Ind.	77221	Phanostrian Instrument and Electronic Co.	South Pasadena, Calif.
26462	Grobet File Co. of America, Inc.	Carlstadt, N. J.	71468	ITT Cannon Electric Inc.	Los Angeles, Calif.	77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
26851	Compac Hollister Co.	Hollister, Calif.	71471	Cinema, Div. Aerovox Corp.	Burbank, Calif.	77342	American Machine & Foundry Co. Potter & Brumfield Div.	Princeton, Ind.
26992	Hamilton Watch Co.	Lancaster, Pa.	71482	C. P. Clare & Co.	Chicago, Ill.	77630	TRW Electronic Components Div.	Camden, N. J.
27251	Specialties Mfg. Co., Inc.	Stratford, Conn.	71590	Centralab Div. of Globe Union Inc.	Milwaukee, Wis.	77638	General Instrument Corp., Rectifier Div.	Brooklyn, N. Y.
28480	Hewlett-Packard Co.	Palo Alto, Calif.	71616	Commercial Plastics Co.	Chicago, Ill.	77764	Resistance Products Co.	Harrisburg, Pa.
28520	Heyman Mfg. Co.	Kenilworth, N. J.	71700	Cornish Wire Co., The	New York, N. Y.	77969	Rubbercraft Corp. of Calif.	Torrance, Calif.
30817	Instrument Specialties Co., Inc.	Little Falls, N. J.	71707	Coto Coil Co., Inc.	Providence, R. I.	78189	Shakeproof Division of Illinois Tool Works	Elgin, Ill.
33173	G. E. Receiving Tube Dept.	Owensboro, Ky.	71744	Chicago Miniature Lamp Works	Chicago, Ill.	78277	Sigma	So. Braintree, Mass.
35434	Lectrohm Inc.	Chicago, Ill.	71785	Cinch Mfg. Co., Howard B. Jones Div.	Chicago, Ill.	78283	Signal Indicator Corp.	New York, N. Y.
36196	Stanwyck Coil Products Ltd.	Hawkesbury, Ontario, Canada	71984	Dow Corning Corp.	Midland, Mich.	78290	Struthers-Dunn Inc.	Pitman, N. J.
36287	Cunningham, W. H. & Hill, Ltd.	Toronto Ontario, Canada	72136	Electro Motive Mfg. Co., Inc.	Williamantic, Conn.	78424	Specialty Leather Prod. Co.	Newark, N. J.
37942	P. R. Mallory & Co. Inc.	Indianapolis, Ind.	72619	Dialight Corp.	Brooklyn, N. Y.	78452	Thompson-Bremer & Co.	Chicago, Ill.
39543	Mechanical Industries Prod. Co.	Akron, Ohio	72656	Indiana General Corp., Electronics Div.	Keasby, N. J.	78471	Tilly Mfg. Co.	San Francisco, Calif.
40920	Miniature Precision Bearings, Inc.	Keene, N. H.	72699	General Instrument Corp., Cap. Div.	Newark, N. J.	78488	Stackpole Carbon Co.	St. Marys, Pa.
42190	Muter Co.	Chicago, Ill.	72765	Drake Mfg. Co.	Harwood Heights, Ill.	78493	Standard Thomson Corp.	Waltham, Mass.
43990	C. A. Norgren Co.	Englewood, Colo.	72825	Hugh H. Eby Inc.	Philadelphia, Pa.	78553	Tinnerman Products, Inc.	Cleveland, Ohio
44655	Ohmite Mfg. Co.	Skokie, Ill.	72928	Gudeman Co.	Chicago, Ill.	78790	Transformer Engineers	San Gabriel, Calif.
46384	Penn Eng. & Mfg. Corp.	Doylestown, Pa.	72962	Elastic Stop Nut Corp.	Union, N. J.	78947	Ucinite Co.	Newtonville, Mass.
47904	Polaroid Corp.	Cambridge, Mass.	72964	Robert M. Hadley Co.	Los Angeles, Calif.	79136	Waldes Kohinoor Inc.	Long Island City, N. Y.
48620	Precision Thermometer & Inst. Co.	Southampton, Pa.	72982	Erie Technological Products, Inc.	Erie, Pa.	79142	Veeder Root, Inc.	Hartford, Conn.
49956	Microwave & Power Tube Div.	Waltham, Mass.	73061	Hansen Mfg. Co., Inc.	Princeton, Ind.	79251	Wenco Mfg. Co.	Chicago, Ill.
52090	Rowan Controller Co.	Westminster, Md.	73076	H. M. Harper Co.	Chicago, Ill.	79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
52983	Sanborn Company	Waltham, Mass.	73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Calif.	79963	Zierick Mfg. Corp.	New Rochelle, N. Y.
54294	Shallcross Mfg. Co.	Selma, N. C.	73293	Hughes Products Division of Hughes Aircraft Co.	Newport Beach, Calif.	80031	Meppo Division of Sessions Clock Co.	Morristown, N. J.
55026	Simpson Electric Co.	Chicago, Ill.	73445	Amperex Elect. Co.	Hicksville, L. I., N. Y.	80120	Schnitzer Alloy Products Co.	Elizabeth, N. J.
55933	Sonotone Corp.	Elmsford, N. Y.	73506	Bradley Semiconductor Corp.	New Haven, Conn.	80131	Electronic Industries Association. Tube meeting EIA Standards-Washington, DC.	Any brand
55938	Raytheon Co. Commercial Apparatus & Systems Div.	So. Norwalk, Conn.	73559	Carling Electric, Inc.	Hartford, Conn.	80207	Unimax Switch, Div. Maxon Electronics Corp.	Wallingford, Conn.
56137	Spaulding Fibre Co., Inc.	Tonawanda, N. Y.	73586	Circle F Mfg. Co.	Trenton, N. J.	80223	United Transformer Corp.	New York, N. Y.
56289	Sprague Electric Co.	North Adams, Mass.	73682	George K. Garrett Co., Div. MSL Industries Inc.	Philadelphia, Pa.	80248	Oxford Electric Corp.	Chicago, Ill.
59446	Telex Corp.	Tulsa, Okla.	73734	Federal Screw Products Inc.	Chicago, Ill.	80294	Bourns Inc.	Riverside, Calif.
59730	Thomas & Betts Co.	Elizabeth, N. J.	73743	Fischer Special Mfg. Co.	Cincinnati, Ohio	80411	Acro Div. of Robertshaw Controls Co.	Columbus, Ohio
60741	Triplitt Electrical Inst. Co.	Bluffton, Ohio	73793	General Industries Co., The	Elyria, Ohio			
61775	Union Switch and Signal, Div. of Westinghouse Air Brake Co.	Pittsburgh, Pa.	73846	Goshen Stamping & Tool Co.	Goshen, Ind.			

Table 5-3. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
80486	All Star Products Inc.	Defiance, Ohio	86684	Radio Corp. of America, Electronic Comp. & Devices Div.	Harrison, N.J.	95566	Arnold Engineering Co.	Marengo, Ill.
80509	Avery Label Co.	Monrovia, Calif.	86928	Seastrom Mfg. Co.	Glendale, Calif.	95712	Dage Electric Co., Inc.	Franklin, Ind.
80583	Hammarlund Co., Inc.	Mars Hill, N.C.	87034	Marco Industries	Anaheim, Calif.	95984	Siemon Mfg. Co.	Wayne, Ill.
80640	Stevens, Arnold, Co., Inc.	Boston, Mass.	87216	Philco Corporation (Lansdale Division)	Lansdale, Pa.	95987	Weckesser Co.	Chicago, Ill.
80813	Dimco Gray Co.	Dayton, Ohio	87473	Western Fibrous Glass Products Co.	San Francisco, Calif.	96067	Microwave Assoc., West Inc.	Sunnyvale, Calif.
81030	International Instruments Inc.	Orange, Conn.	87664	Van Waters & Rogers Inc.	San Francisco, Calif.	96095	Hi-Q Div. of Aerovox Corp.	Olean, N.Y.
81073	Grayhill Co.	LaGrange, Ill.	87930	Tower Mfg. Corp.	Providence, R.I.	96256	Thordarson-Meissner Inc.	Mt. Carmel, Ill.
81095	Triad Transformer Corp.	Venice, Calif.	88140	Cutler-Hammer, Inc.	Lincoln, Ill.	96296	Solar Manufacturing Co.	Los Angeles, Calif.
81312	Winchester Elec. Div. Litton Ind., Inc.	Oakville, Conn.	88220	Gould-National Batteries, Inc.	St. Paul, Minn.	96306	Microswitch, Div. of Minn.-Honeywell	Freeport, Ill.
81349	Military Specification		88698	General Mills, Inc.	Buffalo, N.Y.	96330	Carlton Screw Co.	Chicago, Ill.
81483	International Rectifier Corp.	El Segundo, Calif.	89231	Graybar Electric Co.	Oakland, Calif.	96341	Microwave Associates, Inc.	Burlington, Mass.
81541	Airpax Electronics, Inc.	Cambridge, Maryland	89473	G.E. Distributing Corp.	Schenectady, N.Y.	96501	Excel Transformer Co.	Oakland, Calif.
81860	Barry Controls, Div. Barry Wright Corp.	Watertown, Mass.	89665	United Transformer Co.	Chicago, Ill.	96733	San Fernando Elect. Mfg. Co.	San Fernando, Calif.
82042	Carter Precision Electric Co.	Skokie, Ill.	90030	United Shoe Machinery Corp.	Beverly, Mass.	96881	Thomson Ind. Inc.	Long Is., N.Y.
82047	Spartan Faraday Inc., Copper Hewitt Electric Div.	Hoboken, N.J.	90179	US Rubber Co., Consumer Ind. & Plastics Prod. Div.	Passaic, N.J.	97464	Industrial Retaining Ring Co.	Irvine, N.J.
82116	Electric Regulator Corp.	Norwalk, Conn.	90970	Bearing Engineering Co.	San Francisco, Calif.	97539	Automatic & Precision Mfg.	Englewood, N.J.
82142	Jeffers Electronics Division of Speer Carbon Co.	Du Bois, Pa.	91146	ITT Cannon Elect. Inc., Salem Div.	Salem, Mass.	97979	Reon Resistor Corp.	Yonkers, N.Y.
82170	Fairchild Camera & Inst. Corp. Space & Defense System Div.	Paramus, N.J.	91260	Connor Spring Mfg. Co.	San Francisco, Calif.	97983	Litton System Inc., Adler-Westrex Commun. Div.	New Rochelle, N.Y.
82209	Maguire Industries, Inc.	Greenwich, Conn.	91345	Miller Dial & Nameplate Co.	El Monte, Calif.	98141	R-Tronics, Inc.	Jamaica, N.Y.
82219	Sylvania Electric Prod. Inc. Electronic Tube Division	Emporium, Pa.	91418	Radio Materials Co.	Chicago, Ill.	98159	Rubber Teck, Inc.	Gardena, Calif.
82376	Astron Corp.	East Newark, Harrison, N.J.	91506	Augat Inc.	Attleboro, Mass.	98220	Hewlett-Packard Co., Moseley Div.	Pasadena, Calif.
82389	Switchcraft, Inc.	Chicago, Ill.	91637	Dale Electronics, Inc.	Columbus, Nebr.	98278	Microdot, Inc.	So. Pasadena, Calif.
82647	Metals & Controls Inc. Spencer Products	Attleboro, Mass.	91662	Elco Corp.	Willow Grove, Pa.	98291	Sealectro Corp.	Mamaroneck, N.Y.
82768	Phillips-Advance Control Co.	Joliet, Ill.	91737	Gremar Mfg. Co., Inc.	Wakefield, Mass.	98376	Zero Mfg. Co.	Burbank, Calif.
82866	Research Products Corp.	Madison, Wis.	91827	K F Development Co.	Redwood City, Calif.	98410	Etc Inc.	Cleveland, Ohio
82877	Rotron Mfg. Co., Inc.	Woodstock, N.Y.	91886	Malco Mfg. Co., Inc.	Chicago, Ill.	98731	General Mills Inc., Electronics Div.	Minneapolis, Minn.
82893	Vector Electronic Co.	Glendale, Calif.	91929	Honeywell Inc., Micro Switch Div.	Freeport, Ill.	98734	Paeco Div. of Hewlett-Packard Co.	Palo Alto, Calif.
83014	Hartwell Corp.	Los Angeles, Calif.	91961	Nahm-Bros. Spring Co.	Oakland, Calif.	98821	North Hills Electronics, Inc.	Glen Cove, N.Y.
83058	Carr Fastener Co.	Cambridge, Mass.	92180	Tru-Connector Corp.	Peabody, Mass.	98978	International Electronic Research Corp.	Burbank, Calif.
83086	New Hampshire Ball Bearing, Inc.	Peterborough, N.H.	92367	Elgett Optical Co. Inc.	Rochester, N.Y.	99109	Columbia Technical Corp.	New York, N.Y.
83125	General Instrument Corp., Capacitor Div.	Darlington, S.C.	92607	Tensolite Insulated Wire Co., Inc.	Tarrytown, N.Y.	99313	Varian Associates	Palo Alto, Calif.
83148	ITT Wire and Cable Div.	Los Angeles, Calif.	92702	IMC Magnetics Corp.	Wesbury Long Island, N.Y.	99378	Atlee Corp.	Winchester, Mass.
83186	Victory Eng. Corp.	Springfield, N.J.	92966	Hudson Lamp Co.	Kearney, N.J.	99515	Marshall Ind., Capacitor Div.	Monrovia, Calif.
83298	Bendix Corp., Red Bank Div.	Red Bank, N.J.	93332	Sylvania Electric Prod. Inc. Semiconductor Div.	Woburn, Mass.	99707	Control Switch Division, Controls Co. of America	El Segundo, Calif.
83315	Hubbell Corp.	Mundelein, Ill.	93369	Robbins & Myers Inc.	Palisades Park, N.J.	99800	Delevan Electronics Corp.	East Aurora, N.Y.
83324	Rosan Inc.	Newport Beach, Calif.	93410	Stemco Controls, Div. of Essex Wire Corp.	Mansfield, Ohio	99848	Wilco Corporation	Indianapolis, Ind.
83330	Smith, Herman H., Inc.	Brooklyn, N.Y.	93632	Waters Mfg. Co.	Culver City, Calif.	99928	Branson Corp.	Whippany, N.J.
83332	Tech Labs	Palisades Park, N.J.	93929	G.V. Controls	Livingston, N.J.	99934	Renbrandt, Inc.	Boston, Mass.
83385	Central Screw Co.	Chicago, Ill.	94137	General Cable Corp.	Bayonne, N.J.	99942	Hoffman Electronics Corp. Semiconductor Div.	El Monte, Calif.
83501	Gavitt Wire and Cable Co. Div. of Amerace Corp.	Brookfield, Mass.	94142	Phelps Dodge	Yonkers, N.Y.	99957	Technology Instrument Corp. of Calif.	Newbury Park, Calif.
83594	Burroughs Corp. Electronic Tube Div.	Plainfield, N.J.	94144	Raytheon Co., Comp. Div., Ind. Comp. Operations	Quincy, Mass.	THE FOLLOWING HP VENDORS HAVE NO NUMBER ASSIGNED IN THE LATEST SUPPLEMENT TO THE FEDERAL SUPPLY CODE FOR MANUFACTURERS HANDBOOK.		
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83777	Model Eng. and Mfg., Inc.	Huntington, Ind.	94154	Wagner Elect. Corp., Tung-Sol Div.	Newark, N.J.			
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83942	Aeronautical Inst. & Radio Co.	Lodi, N.J.	94222	South Chester Corp.	Chester, Pa.			
84171	Arco Electronics Inc.	Great Neck, N.Y.	94330	Wire Cloth Products, Inc.	Bellwood, Ill.			
84396	A.J. Glesener Co., Inc.	San Francisco, Calif.	94375	Automatic Metal Products Co.	Brooklyn, N.Y.			
84411	TRW Capacitor Div.	Ogallala, Neb.	94682	Worcester Pressed Aluminum Corp.	Worcester, Mass.			
84970	Sarkes Tarzian, Inc.	Bloomington, Ind.	94696	Magnecraft Electric Co.	Chicago, Ill.			
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85471	A.B. Boyd Co.	San Francisco, Calif.	95236	Allies Products Corp.	Dania, Fla.	0000Z	Willow Leather Products Corp.	Newark, N.J.
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86579	Precision Rubber Products Corp.	Dayton, Ohio	95354	Methode Mfg. Co.	Rolling Meadows, Ill.	000QQ	Cooltron	Oakland, Calif.
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**MANUAL SUPPLEMENT
DIAGNOSTIC PROGRAM PROCEDURES**

for

12607A

DIRECT MEMORY ACCESS

(HP 2114B COMPUTER ACCESSORY KIT)

Note

This manual is considered part of and should be attached to the 12607A Direct Memory Access Option Operating and Service Manual.

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DIAGNOSTIC PROGRAM

12607A DIRECT MEMORY ACCESS

(HP 2114B COMPUTER)

MS-1. INTRODUCTION

MS-2. The diagnostic programs for the 12607A Direct Memory Access Option of the HP 2114B Computer consist of two programs:

- a. 2114B DMA General Diagnostic
- b. 2114B DMA Rate and Transfer Diagnostic

MS-3. The first test confirms the DMA's ability to transfer data accurately from all memory locations, clear and set various peripheral device control bits and perform input/output functions related to Direct Memory Access.

MS-4. The second test establishes the accuracy of DMA data transfer and verifies the DMA function which holds the computer in the 'Execute' phase while data is input to memory (cycle stealing).

MS-5. 2114B DMA GENERAL DIAGNOSTIC

MS-6. HARDWARE CONFIGURATION

MS-7. This program is written for a 2114B computer (4K or 8K memory) with a buffered teleprinter (Model 12531B) and/or a micro-circuit register (MCR) with all other I/O cards removed. The diagnostic package will operate with an MCR or with a teleprinter. If a teleprinter is not used, certain tests are modified or omitted which lead to incomplete testing of the DMA option. The program itself will abort if one of two output devices is not included as part of the hardware setup.

MS-8. The ideal hardware configuration includes both a teleprinter to report errors and program status and MCR to aid in transferring data to and from the computer. In this mode, system input/output (SIO) is configured on the teleprinter channel and the diagnostics are run on the remaining channels. As each channel is checked, the MCR must be moved to a new channel until the teleprinter channel is the only one remaining to be tested. At this point the teleprinter must be configured with the SIO on a different channel (any channel may be used) in order to test the remaining channel.

MS-9. Without an MCR, each channel (10-16) must be configured with the SIO and checked using the teleprinter. Data transfers must be confirmed by using the paper tape punch/reader. (See MS-14. OPERATING PROCEDURES.)

MS-10. FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

MS-11. In order to tailor the diagnostic to his particular needs, the operator may specify several options for program execution by means of the switch register (as shown in table MS-1).

Table MS-1. Switch Register Characteristics

SWITCH REGISTER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWITCH								FUNCTION							
0-5								Select code for the I/O channel containing the MCR (or the teleprinter if no MCR is available).							
6								Set if no teleprinter is available. Clear if teleprinter is available.							
7								Set if no MCR is available. Clear if MCR is available.							
8-9								Spares							
10								Set if error halts are to be omitted.							
11								If set, each diagnostic test runs and halts (with the appropriate message on the teleprinter). This allows the operator to continue to the next test or repeat the current test by setting bit 14.							
12								If set, bit 12 of the switch register turns on or off after each cycle through the complete diagnostic. This indicates that the program has not looped-up and that the tests are being executed.							
13								If set, all type-out is suppressed. If cleared, type-out continues.							
14								If set, the current test recycles instead of advancing to the next test within the diagnostic. If clear, the program automatically advances to the next test within the diagnostic.							
15								If set, program recycles the entire diagnostic and omits the PRESET test. If clear, the program halts with the appropriate message on the teleprinter for the PRESET test and halts at the end of the diagnostic itself. If no MCR is available, setting bit 15 omits the memory address register test and the input/output data transfer tests.							

MS-12. PROGRAM ORGANIZATION

MS-13. Figure MS-1 is a macro flow chart of the diagnostic subroutines and their execution. Each diagnostic subroutine will be described briefly.

SUBROUTINE	FUNCTION
T.BIO	Confirms the ability to set, clear and test the DMA flag and the DMA interrupt capability. This section includes the PRESET Test.
T.WC	Tests the ability of the DMA to set and read the word count register for all numbers.
T.WCR	Tests the word count increment function (rollover) by setting the word count to minus one and forcing a data transfer which should cause the DMA to interrupt.
T.AR	Tests the memory address register by making a DMA output transfer from every location in memory.
T.STC	Tests the DMA function which sets a device control bit when the STC (set control) decision flip-flop is set.
T.CLC	Tests the DMA function which clears a device control bit when the CLC (clear control) decision flip-flop is set.
T.DTO	Tests the DMA data output capability with all possible data patterns.
T.DTI	Tests the DMA data input capability with the same data patterns used in the T.DTO test.
T.DIO	Tests the DMA input/output block transfer capability via the teleprinter punch.

MS-14. OPERATING PROCEDURES

MS-15. The 2114B DMA General Diagnostic is run according to the following instructions:

a. If an MCR is to be used, insert MCR board no. 12566A-M1 or 12566A-M2 into the I/O channel assigned to the DMA (10-16). The MCRs should have the following jumpers:

W1 - B W3 - A W5 - IN W7 - IN
W2 - A W4 - B W6 - IN W8 - IN

b. If a 16-bit Duplex Register (12554A or 12554A-01) replaces the MCR Register, the Register should have the following jumpers:

W1 - IN W3 - IN W5 - A W7 - A
W2 - IN W4 - A W6 - B

c. If any of the four boards listed above are used, they must be interconnected on the 48-pin edge as follows:

A - 1	P - 13
B - 2	R - 14
C - 3	S - 15
D - 4	T - 16
E - 5	U - 17
F - 6	V - 18
H - 7	W - 19
J - 8	X - 20
K - 9	Y - 21
L - 10	Z - AA - 22 - 23
M - 11	BB - 24
N - 12	

Use the 24-pin edge connector 1251-0332 with pin 22 shorted to pin 23. All I/O channels preceding the MCR require either cards or a priority jumper.

d. After the hardware is ready, follow the steps listed below:

1. Load the DMA diagnostic program using the Basic Binary Loader.
2. Load Address 000100₈.
3. Set the switch register bits 0-5 to the select code of the I/O channel containing the MCR. If the MCR is not available, set bits 0-5 to the I/O channel select code of the teleprinter.
4. If the teleprinter is not available, set switch register bit 6.
5. If the MCR or Duplex Register is not available, set switch register bit 7.
6. Refer to table MS-1 and enter any other options desired by means of the switch register.
7. Press RUN.

e. If the teleprinter is being used, a message will be typed when the program has advanced to the PRESET test.

1. Press PRESET.
2. Press RUN.

f. If the MCR is the sole output device and the computer halts with 102011 in the T-Register:

1. Press PRESET.
2. Press RUN.

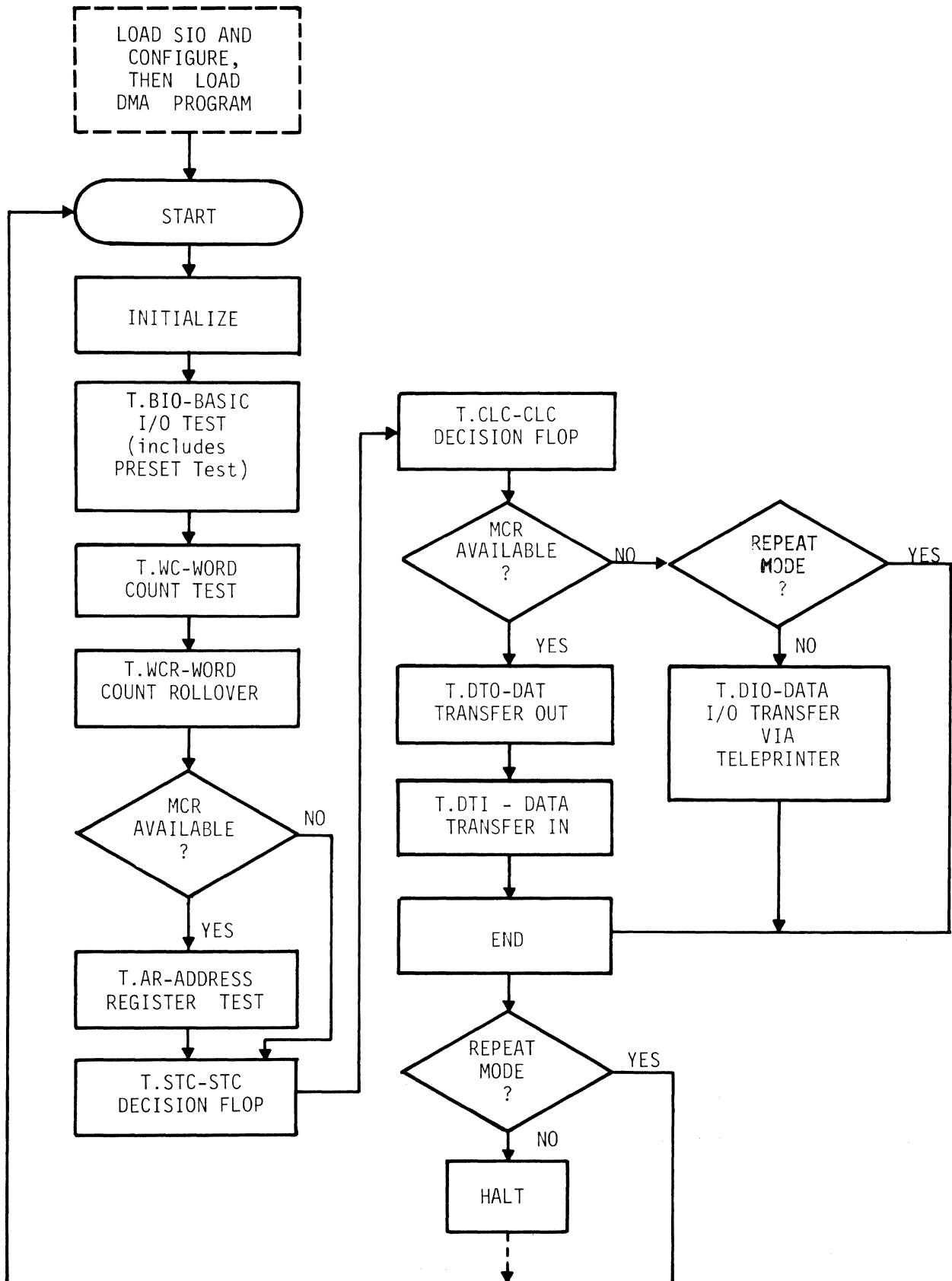


Figure MS-1. HP 2114B DMA General Diagnostic Flowchart

g. An appropriate message indicating the end of the diagnostic will be printed on the teleprinter if it is part of the hardware setup.

h. If an MCR is not used, the teleprinter will type a message, punch a tape and halt. The operator must load the tape reader with the tape punched by the teleprinter and push RUN. The program will read the tape and continue the test.

Note that the continuous feature (bit 15 of the switch register set) will omit this test.

i. If any error halts occur during this program, consult paragraph MS-16.

MS-16. ERROR ANALYSIS SECTION

MS-17. Whenever an error occurs during the execution of the diagnostic program, the computer halts with a coded message in the T-Register. If the teleprinter is included in the hardware configuration, appropriate messages prefixed with an error number (i.e., E12) are typed. Whenever the computer halts, the operator should consult table MS-2 for interpretation. All errors and program status messages are listed opposite the T-Register code and error number.

MS-18. 2114B DMA RATE AND TRANSFER DIAGNOSTIC

MS-19. HARDWARE CONFIGURATION

MS-20. The DMA Rate and Transfer Diagnostic Test requires a 2114B computer (4K or 8K memory) with certain hardware modifications. On the DMA card are four pins: T1, T2, T3, and T4. To run the rate test, T1 should be connected to T2, and T3 should be connected to T4. Neither a teleprinter nor a micro-circuit register is required to run the diagnostic.

MS-21. FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

MS-22. The DMA Rate and Transfer Test verifies that the DMA steals every cycle and transfers data to all of memory. If any errors occur, the program will halt with a coded error message in the T-Register. Each time the program recycles completely, the extend register (which consists of one bit) will blink on or off (complement itself) to indicate that the program is not looping up. There are no options available for this program, and the test, once started, will continue to recycle until either an error condition or the operator halts the program.

MS-23. PROGRAM ORGANIZATION

MS-24. Figure MS-2 is a macro flow chart of the 2114B DMA Rate Test. The program consists primarily of one major test. The operator has no control over any particular section of the program.

MS-4

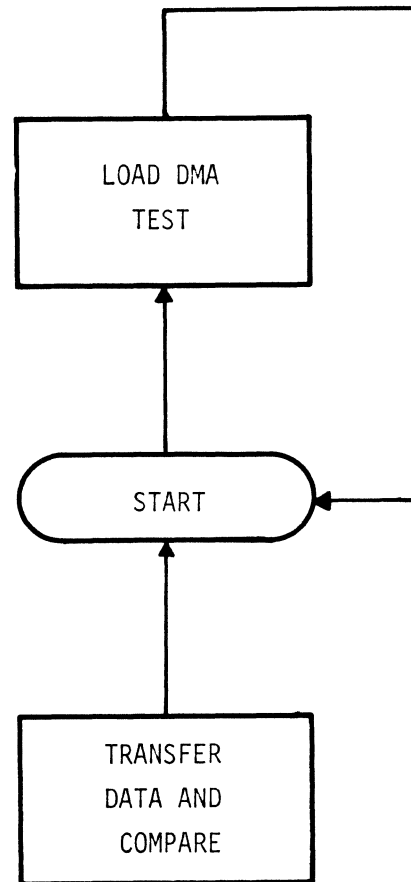


Figure MS-2. DMA Rate and Transfer Test Flowchart

MS-25. OPERATING INSTRUCTIONS

- a. Turn computer power OFF.
- b. Remove the DMA board (slot A16) and short pin T1 to T2, and pin T3 to T4.
- c. Reinsert the DMA board into slot A16, and turn on the computer power.
- d. Load the DMA Rate Test using the Basic Binary Loader.
- e. Load Address 000002₈.
- f. Press PRESET.
- g. Press RUN.

MS-26. The Rate Test should run continuously until an error is detected. After each successful cycle of the test, the E-Register will complement. If an error does occur, the appropriate message will be given in the T-Register. Table MS-3 explains the T-Register error messages.

Table MS-2. DMA General Diagnostic Test Errors and Messages

<u>T-REGISTER</u>	<u>ERROR NO.</u>	<u>MESSAGE</u>	<u>COMMENTS</u>
1060XX	(none)	(none)	Trap cell interrupt. P = memory address when interrupted, XX = the trap cell location.
102001	E1	(none)	The diagnostic must have a teleprinter and/or a MCR for a minimum hardware configuration (test aborted).
102002	E2	E2. CLF DID NOT CLEAR FLAG, OR SFS CAUSED SKIP WITH FLAG CLEAR.	Test the ability to clear the DMA flag and test the SFS instruction.
102003	E3	E3. SFC DID NOT SKIP WITH FLAG CLEAR.	Test the ability of the SFC instruction.
102004	E4	E4. STF DID NOT SET FLAG, OR SFC CAUSED SKIP WITH SET.	Test the ability to set the DMA flag and test the SFC instruction.
102005	E5	E5. SFS DID NOT SKIP WITH FLAG SET.	Test the ability of the SFS instruction.
102006	E6	E6. DID NOT INTERRUPT.	Test the DMA interrupt capability.
102007	E7	E7. THE RETURN ADDRESS (STORED IN A REG.) IS NOT CORRECT.	Test the return address that was placed in the DMA trap cell.
102010	E10	E10. CENTRAL INTERRUPT FUNCTION FAILED.	Test the central interrupt register for an indication that the DMA interrupted.
102011	E11	E11. PRESS PRESET. THEN PRESS RUN.	Checks that the PRESET switch will set the DMA flag. This is not an error.
102012	E12	E12. PRESET DID NOT SET THE DMA FLAG.	The test failed.
102013	(none)	END T.BIO	Select options and press RUN.
102020	E20	E20. WORD COUNT READBACK FROM DMA NOT THE SAME AS OUTPUT WORD. WORD COUNT IS XXXXX AND SHOULD BE XXXXX.	Tests the ability to set and read the word count register.
102021	(none)	(none)	Same message as 20 (with no teleprinter). Switch register contains the word which was output. Press RUN to display the word read back.
102022	(none)	(none)	Switch register contains the word read back from the DMA. Press RUN to continue test.
102023	(none)	END T.WC	Select options and press RUN.

Table MS-2. DMA General Diagnostic Test Errors and Messages (Continued)

<u>T-REGISTER</u>	<u>ERROR NO.</u>	<u>MESSAGE</u>	<u>COMMENTS</u>
102025	E25	E25. DMA TRANSFER SHOULD BE FINISHED.	Checks the word count rollover by setting the word count to minus one and forcing a transfer. This should cause the DMA to interrupt before reaching this halt.
102026	E26	E26. DMA WORD COUNT ROLL-OVER IS XXXXXX AND SHOULD BE 000000.	Same test as E25. The DMA word count roll-over should be zero.
102027	E27	E27. DMA DID NOT INTERRUPT FROM THE CORRECT PLACE. INTERRUPT LOCATION IS XXXXX AND SHOULD BE XXXXX.	Same test as E25, E26. DMA is not interrupting from the correct location.
102030	(none)	(none)	Same message as E27 (with no teleprinter). Switch register contains the expected interrupt location. Press RUN to display the actual interrupt location.
102031	(none)	(none)	Switch register contains the actual interrupt location. Press RUN to continue test.
102032	(none)	END T.WCR	Select options and press RUN.
102035	E35	E35. DMA FLAG SHOULD BE SET.	Tests the memory address register by making a DMA output transfer from every available location in memory. The DMA flag is not set after the data transfer.
102036	E36	E36. WORD READ FROM MICRO-CIRCUIT REGISTER NOT CORRECT WORD IS XXXXXX AND SHOULD BE XXXXXX AND MEM. ADD IS XXXXXX.	Same test as E35 except that the data read is not the same as the data sent. This indicates that the data transfer may be bad or that the DMA is not transferring data from every memory location.
102037	(none)	(none)	Same message as E36 (with no teleprinter). Switch register contains the expected output word. Press RUN to display the word read from the MCR.
102040	(none)	(none)	Switch register contains the MCR. Press RUN to display the memory address.
102041	(none)	(none)	Switch register contains the memory address from which the transfer was executed. Press RUN to continue the test.
102042	(none)	END T.AR	Select options and press RUN.

Table MS-2. DMA General Diagnostic Test Errors and Messages (Continued)

<u>T-REGISTER</u>	<u>ERROR NO.</u>	<u>MESSAGE</u>	<u>COMMENTS</u>
102043	E43	E43. DEVICE CONTROL BIT NOT SET BY DMA WHEN STC DECISION FLOP SET.	Tests the STC decision flip-flop. The DMA should set the device control bit when the STC decision flip-flop is set.
102044	E44	E44. DEVICE CONTROL BIT SET BY DMA WHEN STC DECISION FLOP CLEAR.	Tests the STC decision flip-flop. The DMA should not set the device control bit when the STC decision flip-flop is clear.
102045	(none)	END T.STC	Select options and press RUN.
102046	E46	E46. DEVICE CONTROL BIT NOT CLEARED BY DMA AT END OF BLOCK TRANSFER WHEN CLC DECISION FLOP SET.	Tests the CLC decision flip-flop. The DMA should clear the device control bit during the last transfer of a block when the CLC decision flip-flop is set.
102047	E47	E47. DEVICE CONTROL BIT CLEARED BY DMA WHEN CLC DECISION FLOP CLEAR.	Test the CLC decision flip-flop. The DMA should not clear the device control bit when the CLC decision flip-flop is clear. The DATA pattern (10670XX) output may have caused the device control to be cleared on ring phase 5. The A14 assembly (shift logic card) must be 02114-6003 version B or later.
102050	(none)	END T.CLC	Select option and press RUN.
102051	E51	E51. DMA FLAG SHOULD BE SET.	Test all possible patterns in the DMA data output capability. The DMA flag is not set after data transfer.
102052	E52	E52. DATA PATTERN READ BACK FROM MCR NOT THE SAME AS THAT OUTPUT BY DMA. PATTERN IS XXXXXX AND SHOULD BE XXXXXX.	Same test as E51 except that the data pattern transferred is in error.
102053	(none)	(none)	Same message as E52 (with no teleprinter). Switch register contains the word output by the DMA. Press RUN to display the word read back from the MCR.
102054	(none)	(none)	Switch register contains the word read back from the MCR. Press RUN to continue test.
102055	(none)	END T.DTO	Select options and press RUN.
102056	E56	E56. DMA FLAG SHOULD BE SET.	Tests all possible data patterns of the DMA input transfer capability. The DMA flag is not set after the data transfer.

Table MS-2. DMA General Diagnostic Test Errors and Messages (Continued)

<u>T-REGISTER</u>	<u>ERROR NO.</u>	<u>MESSAGE</u>	<u>COMMENTS</u>
102057	E57	E57. DATA PATTERN READ BACK FROM THE SAME AS THAT OUTPUT BY MCR. PATTERN IS XXXXXX AND SHOULD BE XXXXXX.	Same test as E56 except that the data pattern transferred is in error.
102060	(none)	(none)	Same message as E57 (with no teleprinter). Switch register contains the word output from the MCR to the DMA. Press RUN to display the word input from the DMA.
102061	(none)	(none)	Switch register contains the word input from the DMA. Press RUN to continue tests.
102062	(none)	END T.DTI	Select options and press RUN.
102064	(none)	(none)	The DMA flag did not set after the transfer of data (this is a timed test).
102065	E65	E65. DATA PATTERN READ IN FROM READER IS NOT THE SAME AS THAT OUTPUT TO PUNCH. PATTERN IS XXXXXX AND SHOULD BE XXXXXX.	Same test as E64 except that the data pattern transferred is in error.
102066	(none)	END T.DIO	Select options and press RUN.
102077	E77	E77. DMA DIAGNOSTIC PROGRAMS HAVE BEEN EXECUTED. TELE-PRINTER USED FOR DATA TRANSFER.	Not an error message. Select options and press RUN to recycle the DMA diagnostic programs.

Table MS-3. DMA Rate and Transfer Diagnostic Test Errors and Messages

<u>T-REGISTER</u>	<u>TEST DESCRIPTION</u>
XXXXXX	If the program halts with any number in the T-Register other than the three listed below and any number other than 000044 in the M-Register, the DMA is not stealing every cycle.
102070	An incorrect data transfer has taken place. The switch register contains the correct data. Press RUN to display the incorrect data.
102071	The incorrect data referenced by the above halt is now stored in the switch register. Press RUN to continue.
102072	The DMA did not transfer the data when instructed, or it did transfer the data but did not interrupt as expected.